Carbon nanomaterials for non-volatile memories

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Abstract | Carbon can create various low-dimensional nanostructures with remarkable electronic, optical, mechanical and thermal properties. These features make carbon nanomaterials especially interesting for next-generation memory and storage devices, such as resistive random access memory, phase-change memory, spin-transfer-torque magnetic random access memory and ferroelectric random access memory. Non-volatile memories greatly benefit from the use of carbon nanomaterials in terms of bit density and energy efficiency. In this Review, we discuss sp^2-hybridized carbon-based low-dimensional nanostructures, such as fullerene, carbon nanotubes and graphene, in the context of non-volatile memory devices and architectures. Applications of carbon nanomaterials as memory electrodes, interfacial engineering layers, resistive-switching media, and scalable, high-performance memory selectors are investigated. Finally, we compare the different memory technologies in terms of writing energy and time, and highlight major challenges in the manufacturing, integration and understanding of the physical mechanisms and material properties.

Solid-state non-volatile memories (NVMs) have greatly improved the speed and energy efficiency of modern computing systems in the past decade owing to data storage properties superior to those of the magnetic hard disk drives that have been in use since the 1950s. NAND flash[1] is the mainstream NVM device of the modern electronics era. The floating-gate transistor structure of NAND flash has now reached its fundamental scaling limit of very few (10–20) storage electrons, and this technology faces substantial variability and reliability concerns, such as limited endurance cycles. This makes it difficult to fulfil the application requirements for NVM devices to be scaled down in 2D for technology nodes smaller than 1z nm (~13 nm)[2,3]. Advances in 3D NAND technology have enabled continued density scaling by employing charge trapping[4] and other bit-cost scalable (BiCS) techniques[5] that provide high device areal density through the use of the third dimension. An example is the recent development of Western Digital's fourth-generation 3D NAND chips that feature a storage capacity of 1 Tb with 96 layers in 3D[6]. However, there are manufacturing and fabrication challenges to advance NAND technologies in 3D, and the number of device layers for 3D NAND is expected to be practically limited to approximately 128 layers[7]. In view of this and the strong demand for higher-capacity memories (especially, memories that can be co-located with the computation elements)[8], nanoscale random access memories (RAMs) that are based on hysteretic resistance changes[9–11], such as resistive RAM (RRAM)[12–20], phase-change memory (PCM)[21–26], spin-transfer-torque magnetic RAM (STT-MRAM)[27–31], and ferroelectric RAM (fRAM)[32–36], have gained great attention in the field.

Unlike flash, RRAM has a simple two-terminal structure consisting of a transition metal oxide sandwiched between two metal electrodes[19,20], with excellent scalability below 10 nm (REF. 37). RRAM is thus a promising candidate to complement NAND flash as a BiCS technology for mass storage applications. The switching mechanism is governed by the formation and rupture of a conductive filament by migrating oxygen ions (metal-oxide RAM)[16,19] or high-mobility metal electrode ions (conductive-bridge RAM)[16,18]. PCM, another important class of nanoscale data storage technology, uses Joule-heating-induced reversible switching between the low-resistance crystalline and high-resistance amorphous phases of chalcogenide alloys[22,26]. This technology is more mature than RRAM, and large-scale chips[24,25] and the first commercial products are already available[38]. Several other NVMs have been designed to combine the benefits of NAND flash (non-volatility) and dynamic RAM (DRAM) (fast speed). For example, in STT-MRAM[28], a spin-polarized current exerts a STT[39,40] to change the magnetization direction of a nanomagnet. The resultant resistance difference can be detected, offering read and write times of a few nanoseconds[41] and a virtually unlimited lifetime of 10^{15} endurance cycles[42]. Everspin Technologies (in partnership with GlobalFoundries) delivered 256 Mb STT-MRAM

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products (with speeds comparable to those of DRAM) in 2016 and has recently announced the sampling of 1 Gb chips with a double data rate fourth-generation (DDR4)-compatible interface[43]. Furthermore, using spin-orbit torque for magnetization switching opens new possibilities to overcome the shortcomings of contemporary STT-MRAM technology[44], such as engineering the trade-off between switching speed and power consumption. fRAM[35,45] is a field-driven NVM technology based on a ferroelectric material that retains its polarization once the electric field is removed. The resultant hysteresis loop of the polarization charge versus voltage is used to store the bi-stable, non-volatile and polarized states ('0' for upward polarization and '1' for downward polarization) in the fRAM cell. Despite having a low density[34], fRAM is a fast, low-power memory that can endure a very high number of programming cycles (up to 10^{14})[46], gaining increasing interest owing to recent advances in non-perovskite ferroelectric materials (for example, ferroelectric hafnium oxide (HfO_x) doped with silicon[47–49], aluminium[50], zirconium[51] or yttrium[52]).

The ability to store terabytes of data with remarkable energy efficiency using NVMs has been made possible through the use of carbon nanomaterials. Carbon is one of the most abundant elements that can exist in various physical forms. sp^2-Hybridized carbon[53,54] forms covalent bonds with high bonding energies of 5.9 eV (REF. 54). In this graphitic form, carbon can create various low-dimensional nanostructures, such as fullerene (C_{60}), carbon nanotubes (CNTs) and graphene. Fullerene consists of 20 hexagonal and 12 pentagonal carbon rings, with each atom strongly bound to three others through sp^2-hybridization. C_{60} behaves like an electron-deficient alkene and therefore readily reacts with electron-rich species, enabling the use of C_{60} as an organic resistive-switching medium for charge transfer together with electron donors. CNTs are cylindrical graphitic sheets that are rolled-up into a seamless cylinder with diameters on the order of 1–4 nm. Graphene is an atomically thin sheet of carbon atoms with a thickness of 0.34 nm. Graphene constitutes an important class of carbon allotropes exhibiting unique 2D hexagonal structures, with numerous applications in NVM research. Research into sp^2-hybridized carbon-based materials[53] has led to their use in many devices, such as wearable strain sensors[55] and a THz wave detector[56,57]. The properties of carbon nanomaterials (TABLE 1) can be exploited to address two crucial issues in NVM technology: scalability (state-of-the-art RRAMs and PCMs are still limited to storage capacities of <100 Gb (REF. 9)) and energy efficiency (the write energies of NVMs are greater than 100 fJ per bit[58]).

This Review discusses carbon nanomaterials in the context of NVM technologies, highlighting their progress, prospects and challenges. We examine how carbon nanomaterials can be integrated with NVMs to develop nanoscale memory systems with advanced capabilities, detailing their use as electrodes, interfacial engineering layers, resistive-switching media, and scalable, high-performance selectors. Finally, the major challenges in terms of manufacturing, device integration and understanding of the physical mechanisms and material properties are discussed.

Carbon nanomaterials as electrodes

Carbon nanomaterials are suitable as nanoscale electrodes for memories without the need to use conventional lithographic techniques because of their nanometre-scale dimensions. RRAM has a simple cell structure and less stringent requirements for electrode materials[19] compared with those of other NVMs (for example, electrodes have to be magnetic materials in STT-MRAM) and has therefore been among the first technologies integrating carbon nanomaterials as crossbar or edge electrodes for ultra-high-density NVMs. Besides offering the opportunity to miniaturize the NVM cell, using carbon nanomaterials as electrodes also enables energy-efficient device operation. For example, the RESET-programming current of a PCM, that is, the current required to program

Table 1 | **Solid-state properties of selected sp^2-hybridized carbon-based low-dimensional nanostructures**

Carbon nanomaterial	Physical dimensions	Optical		Electrical		Mechanical		Thermal
		Band gap (eV)	Transmittance (%)	Mobility ($cm^2(Vs)^{-1}$)	V_{sat} ($cm\,s^{-1}$)	Young's modulus (GPa)	Fracture strain (%)	Conductivity ($(W(mK)^{-1}$)
C_{60}	*d*: 0.7 nm (a single molecule)	1.5–2.3	80–94	0.18–11	NA	53–69 (nanowhisker)	NA	0.2–0.4
CNT (single-wall)	*d*: 1–4 nm, *l*: 10 nm–325 μm	0.2–0.8	86–88	20–79,000	4×10^7 (theory)	1,250	2–19	2,000–3,500
GNR	t: 0.34 nm, *w*: 2–100 nm, *l*: 2 nm–2 μm	0.003–0.4	NA (52–74 in f-GNR)	50–200 (10^1–10^4 in theory)	$2–5\times10^7$	964 (theory)	20 (theory)	70–220
Graphene	*t*: 0.34 nm (monolayer), *A*: 10s of $μm^2$–mm^2	0	98 (monolayer)	3,000–50,000	$4–6\times10^7$	1,000	25	600–3,000
GO	*t*: 2.9–8.5 nm, *A*: 10s of $μm^2$	1 (rGO)–3.5	80–90	0.5–200 (rGO)	NA	200–550	10–22	8.8

The electrical properties were calculated or measured at room temperature. For carbon nanotube (CNT)[183–194] and graphene[195–200], the charge carriers can be either electrons or holes owing to the band symmetry. Hole mobility is experimentally easier to measure because of the better p-type contact metals. For transmittance (%), the 2D thin-film network of CNTs (sheet resistance, R_S, of 200 Ω per square) and graphene nanoribbons (GNRs)[89,201–209] (R_S of 1,500–10^4 Ω per square) were measured in the visible light wavelength range of 500–700 nm. *t*, *d*, *w*, *l* and *A* indicate thickness, diameter, width, length and area of carbon nanomaterials, respectively. C_{60}, fullerene[210–216]; f-GNR, functionalized GNR[224]; GO, graphene oxide[217–223]; NA, not available; rGO, reduced GO; V_{sat}, saturation velocity[225].

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the cell into the RESET or high-resistance state (HRS), scales linearly with the physical cell dimension[26,59]; thus, electrodes at the nanoscale improve the energy efficiency of a PCM device.

Ultra-high-density RRAMs

A large number of materials have been explored as electrodes for RRAM, including elemental metals (Cu, Pt, Al and Au)[60], metal nitrides (titanium nitride (TiN))[61], conductive oxides (indium tin oxide (ITO))[62] and doped silicon[63]. Electrode materials need to be carefully chosen for an RRAM because the device characteristics and switching mechanisms depend on the electrode material[16,19,60]. Ultra-high-density RRAMs with excellent switching behaviour have been realized using carbon nanomaterials as crossbar or edge electrodes.

Carbon nanotube crossbar electrodes. One of the best-studied carbon nanomaterials for RRAM electrodes is CNTs. In addition to their excellent electrical, thermal and mechanical properties[64], which fulfil the general requirements for electrode materials (TABLE 1), their one-dimensionality allows a simple crossbar (or cross-point) structure with the small footprint cell size of $4F^2$ (where F is the width of both lines and spaces for metal lines)[65,66]. The individual memory cell size of the CNT-crossbar RRAM array is limited only by the nanometre-scale CNT diameter. This is an important feature because the metallic electrodes of RRAM arrays are usually fabricated using top-down lithographic processes, which define the active cell area and therefore limit the memory density. Furthermore, the manufacturability of CNTs has been greatly improved in terms of large-scale growth, transfer and device integration[67–72], opening the route towards the fabrication of ultra-high-density RRAMs using CNT electrodes.

Nanoscale RRAMs with CNT-crossbar electrodes were first reported in 2011 (REF. 73) using CNTs with an average diameter of 1.2 nm as one or both RRAM electrodes, achieving a cycling endurance of 10^4 and programming currents of less than 5 µA. For a similar RRAM device using a CNT/aluminium oxide (AlO_x)/CNT stack, a remarkably low switching energy of less than 10 fJ per bit has been estimated using the measured switching currents and voltages and the assumed switching time of 10 ns observed in AlO_x RRAMs[74]. These CNT RRAMs[74] exhibit reasonable SET/RESET voltages of +5.5 V/−3.5 V after the initial forming step at ~8 V (with an imposed current compliance of 1 µA), which is commonly observed for RRAM operations. In the AlO_x-based RRAM using CNT electrodes, a single cross-point memory cell dictates the switching behaviour of devices with tens of cross-points, suggesting that only a single active bit exists at the intersection of the CNT-crossbar electrodes, independent of the number of CNT–CNT junctions[74] (FIG. 1a). The low RESET currents (1–100 nA) occurring in CNT-crossbar electrode devices[74] may be an intrinsic property of AlO_x-based RRAM rather than being attributed to the use of CNTs (FIG. 1b). Interestingly, by using a different metal-oxide material, HfO_x, in an Al/HfO_2/CNT device structure, sub-µA RESET currents

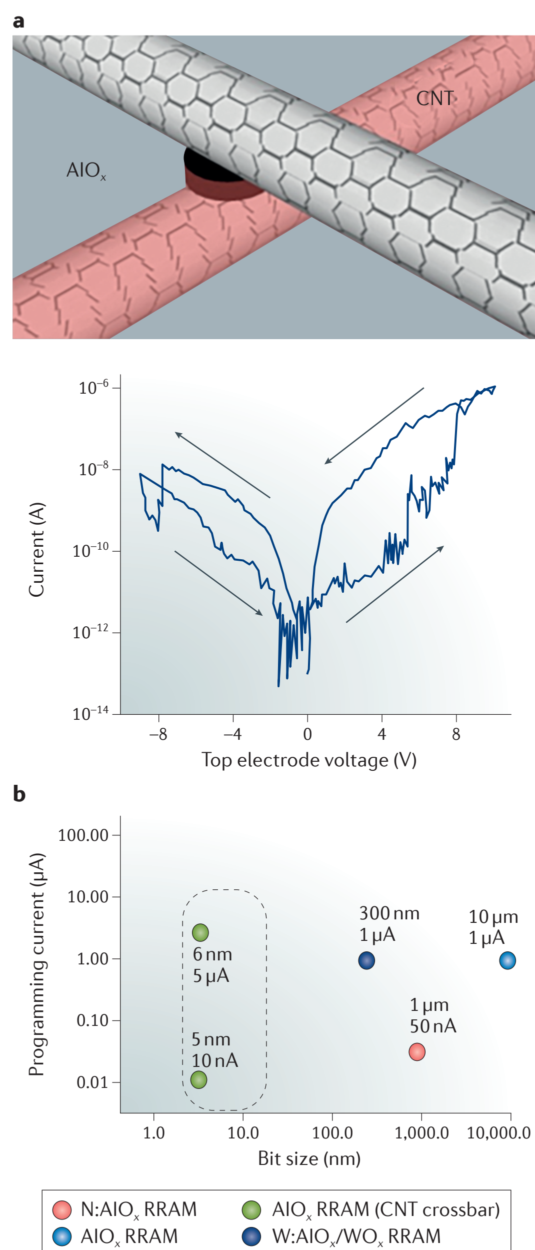

Figure 1 | **Carbon nanotubes as crossbar electrodes.** **a** | Carbon nanotube (CNT) crossbar electrode in an aluminium oxide (AlO_x)-based resistive random access memory (RRAM) (top panel). This device shows excellent switching behaviour of sub-100 nA programming currents (bottom panel)[74]. The use of metallic or semiconducting CNTs as top and bottom electrodes of RRAM cells enables nanoscale RRAM bits with ON/OFF resistance ratios of up to 10^5, programming currents of 1–100 nA and few-volt SET/RESET voltages. **b** | Programming current versus memory bit size for AlO_x-based RRAMs with (green)[73,74] and without (blue, red)[179–181] CNT electrodes. CNT-crossbar electrodes reduce the physical dimension of the RRAM bit to the single-digit nanometre regime while preserving the low-power consumption characteristic of AlO_x-based RRAMs, including W:AlO_x/WO_x (tungsten-doped AlO_x/WO_x bilayer) RRAM and N:AlO_x (nitrogen-doped AlO_x) RRAM. Part **a** is adapted with permission from REF. 74, American Chemical Society.

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(~130 nA) are also obtained[75]. These inconclusive experimental findings reflect the need for further investigations to understand the effects of CNT electrodes on the switching behaviour of RRAMs.

Graphene edge electrodes. Graphene has been used as an electrode material for memory devices because of its superior thermal, chemical and electronic transport characteristics, as well as its sub-nanometre thickness[76–78] (TABLE 1). In RRAMs, the edge of a planar graphene electrode can be in physical contact with the memory switching medium, and such an electrode is called an edge electrode.

3D vertical RRAM is the only technology that can potentially compete with the high-density 3D NAND flash currently in use[79–81], and it has greatly benefited from graphene research[82–84]. The 3D vertical RRAM adopts a BiCS architecture that resembles 3D NAND technology, which is currently the strongest market driver in the semiconductor memory industry. The density of a 3D vertical RRAM array is limited by the sheet resistance and the thickness of the edge electrode, and less by the lithographic half-pitch[80,81] owing to the high electrical resistivity of the planar electrode material (usually made of bulk materials, for example, TiN) and imperfections at the vertical etching angle[80]. Therefore, the thickness of the edge electrode layer determines how many vertical layers can be stacked, and it is a key factor that determines the storage density of a 3D vertical RRAM. In 3D vertical RRAMs, ultrathin graphene can serve as the planar edge electrode at the intersection of the vertical pillar metal electrode and the resistive-switching layers (metal oxides) (FIG. 2a). The thickness (0.34 nm) and sheet resistance (125 Ω per square, doped[77]) of a graphene monolayer are substantially lower than those of any bulk metal of comparable thicknesses, which makes graphene an ideal edge electrode material for 3D vertical RRAMs. A 3D vertical, HfO_x-based RRAM with graphene monolayers as edge electrodes[82] has a low switching energy of approximately 230 fJ and performs 1,600 endurance cycles with ON/OFF resistance ratios (R_{OFF}/R_{ON}) of up to 70 (FIG. 2a).

Low-power phase-change memories

The high programming currents in PCMs[26] prevent the use of PCM technology in applications that require low power consumption and place stringent on-state conduction requirements on the memory selector, which is typically integrated in series with the PCM cell. Therefore, the memory selector needs to have a large area in order to provide high currents, thus limiting the device density of PCM technology. The use of carbon nanomaterials as PCM electrodes is an effective approach to address the issue of high programming currents. In contrast to that of RRAM, the required RESET-programming current of PCM scales with the contact area, that is, between the bottom electrode, which can serve as a 'heater', and the phase-change material in a conventional mushroom structure. Thus, the use of nanoscale electrodes decreases the contact area and therefore the required current.

Carbon nanotube electrodes. The first nanoscale PCM bit cell was demonstrated by creating a nanogap in the middle of the CNT and filling this gap with the sputtered phase-change alloy $Ge_2Sb_2Te_5$ (GST)[85]. Using CNT electrodes, the PCM cells could be scaled down to the single-digit nanometre regime with programming currents of only a few µAs and a required energy of 100 fJ (per bit). By contrast, state-of-the-art PCM technology at that time, which relied on sub-lithographic techniques and cell structures or thermal designs, required two orders of magnitude higher RESET currents (for example, I_{RESET} ~200 µA for F = 45 nm (REF. 26)). CNTs with diameters of a few nanometres can carry large current densities (~1 GA cm^{-2}) and form atomically sharp contacts with the PCM, which are suitable for handling the current densities (~1–10 MA cm^{-2}) needed for programming the PCM[86].

Using CNT as a PCM electrode in a crossbar geometry (replacing only the bottom electrode)[87,88] or using self-aligned PCM nanowires with CNTs[59] for nanoscale PCM cells (FIG. 2b) also reduces the programming current and energy in PCM (FIG. 2c).

Graphene nanoribbon electrodes. Graphene can be patterned into a 1D structure to form a graphene nanoribbon (GNR)[89]. GNRs have been explored as edge electrodes for PCM cells with large contact widths of 30–400 nm or even micrometre scale[90]. Using a similar device geometry as that for CNT-contacted nanoscale PCMs[85], programming currents in a single µA range, threshold voltages as low as ~3 V and R_{OFF}/R_{ON} ratios of ~100 can be achieved[90]. PCM devices in contact with few-layer graphene edges have a power consumption that is approximately an order of magnitude higher than that of devices using CNT electrodes. This difference in power consumption is consistent with the larger contact area between the graphene edges and the PCM cell. Graphene electrodes have been suggested to be better suited than CNT electrodes for large-scale device fabrication[77]. However, as of yet, the GNR-contacted PCM devices have shown only approximately 10 switching cycles[90]. Thus, additional research is required to improve the reliability of such devices through the control of the PCM–graphene interface.

Interfacial engineering layers

Carbon nanomaterials have also been explored as interfacial layers to further elucidate the resistive-switching mechanism of RRAMs, to improve the heating efficiency of PCMs, and to make fRAMs more reliable. Specifically, graphene can easily be integrated with a large-scale complementary metal-oxide semiconductor (CMOS) or other advanced flexible platforms as an interfacial layer in a multilayer NVM device stack, for example, in RRAMs[91,92].

Graphene as oxygen ion probe in RRAM

In an RRAM, monolayer graphene can be inserted at the interface between the top electrode and the resistive-switching layers to monitor and detect the migration of oxygen ions[93] (FIG. 3a); oxygen ion migration is a key process to explain the resistive-switching mechanism in RRAM[19].

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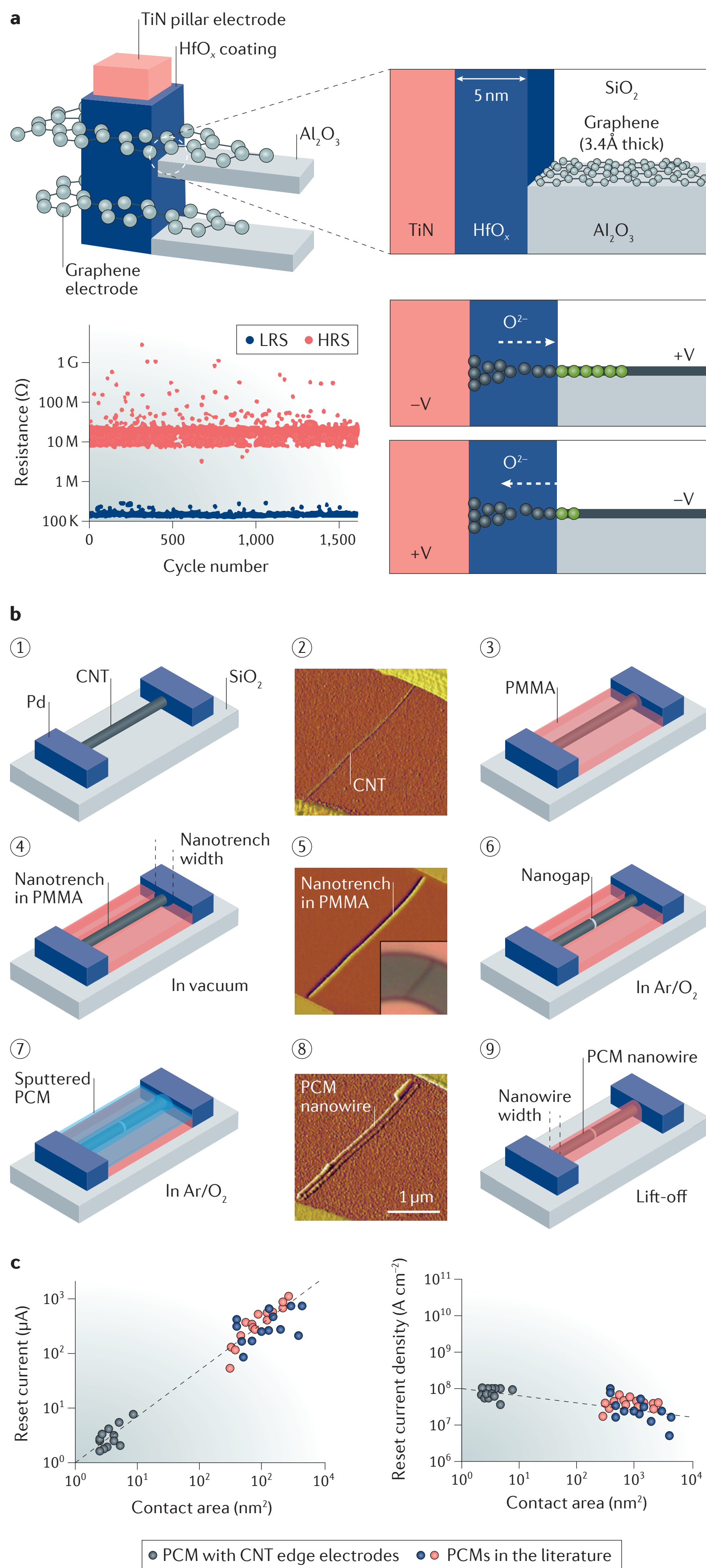

Figure 2 | **Carbon nanomaterials as edge electrodes.** **a** | Schematic of a 3D vertical resistive random access memory (RRAM) with graphene-based edge electrodes (top panel) and a proposed switching mechanism (bottom right panel). Measured endurance characteristics are shown for an RRAM at the low-resistance state (LRS) and high-resistance state (HRS) (bottom left panel)[82]. In contrast to a 3D vertical RRAM with conventional metal thin films as edge electrodes, oxygen ions in the graphene-based RRAM do not accumulate at the edge but horizontally migrate at the graphene/oxide interface (bottom right panel). The measured endurance characteristic of approximately 1,600 cycles (with a 500 ns pulse width) indicates that the quality of the graphene interface can be improved. **b** | Fabrication process for nanoscale ultra-low-power phase-change memory (PCM) bit contacted by carbon nanotube (CNT) edge electrodes[59]. The CNT is contacted by two palladium electrodes on a SiO_2 substrate (1), shown by atomic force microscopy (AFM) (2). The device is then coated with a thin layer (~50 nm) of poly(methyl methacrylate) (PMMA) (3), and the nanotrench (90 nm wide) is formed in vacuum (10^{-5} torr) by Joule heating the CNT (4,5). The CNT nanogap is created by electrical cutting under Ar/O_2 flow (6), and $Ge_2Sb_2Te_5$ (GST) is deposited to fill the nanogap and nanotrench (7). The corresponding AFM image and cartoon show the self-aligned PCM nanowire with the CNT electrodes obtained after PMMA lift-off (8,9). **c** | RESET current and current density versus contact area are shown for CNT-contacted PCM cells[59] and state-of-the-art PCMs, as reported in the literature[26,182]. Part **a** is adapted from REF. 82, Macmillan Publishers Limited. Parts **b** and **c** are adapted with permission from REF. 59, American Chemical Society.

To investigate the resistive-switching mechanism of RRAM, the migration of negatively charged oxygen ions from HfO_x to the top electrode interface (during the SET operation, in which a positive bias voltage is applied to the top electrode) or vice versa (during the RESET operation) can be examined in a non-destructive way by observing the Raman spectral change of the graphene-inserted RRAM device because the presence of oxygen is reflected by a change in the 2D-peak intensity and G-peak position of the Raman spectrum of graphene[94]. During the SET operation, the wavenumber of the G-peak increases (blue shift) and the intensity of the 2D-peak decreases, which can be attributed to the oxygen ions migrating towards the top electrode and then laterally diffusing along the graphene interfacial layer until the formation of covalent bonds with existing defects on the graphene surface[93]. During the RESET operation, with the reverse electric field applied, oxygen ions migrate back to the oxide layer (HfO_x), resulting in a red shift of the G-peak and an increase in 2D-peak intensity. This behaviour is repeatedly observed for many cycles of SET and RESET programming (FIG. 3a). When integrated into an RRAM device stack, graphene might prevent oxygen ions from further migrating deep into the metal electrode (anode), thus potentially improving the reliability by preventing degradation of RRAM devices upon repeated programming cycles[93].

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Graphene in transparent RRAM

Transparent RRAM technology can be enhanced by inserting a graphene monolayer sheet into the interface between a transparent top electrode (composed of ITO) and a ZnO resistive-switching layer[95] (FIG. 3b). The resultant RRAM device shows better switching behaviour with higher switching yield and uniformity than those of the device without graphene. In this case, graphene acts not only as an effective transparent electrode for RRAM[96] but also as a robust passivation layer to ameliorate undesired surface effects, such as band bending[97], chemisorption or photodesorption at the surface[98] and surface roughness[99]. Thereby, the excellent optical properties of carbon nanomaterials can be explored for the field of transparent electronics, which could prove beneficial for innovative memory products, such as an infotainment system displayed on an automobile windshield.

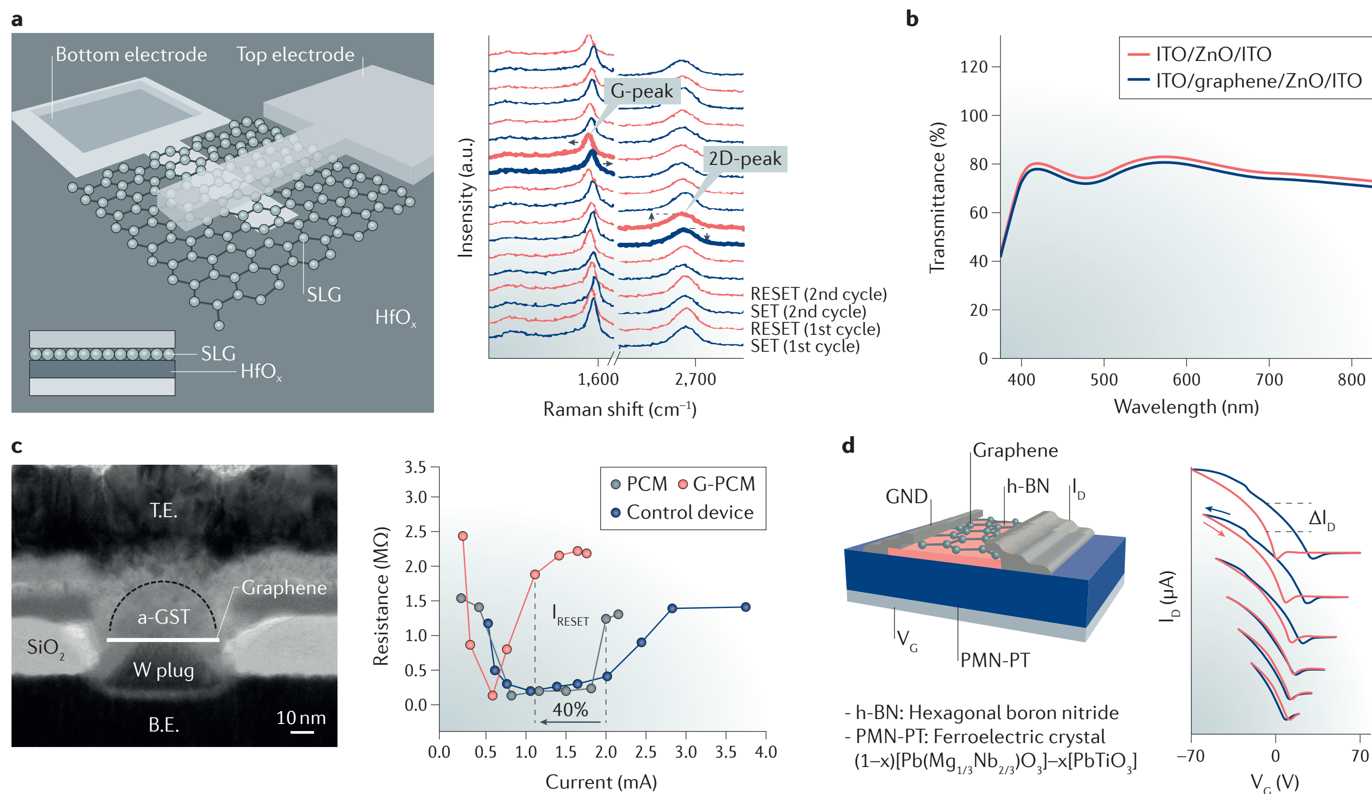

Figure 3 | **Graphene as an interfacial engineering layer. a** | Single-layer graphene (SLG) can be inserted at the hafnium oxide (HfO_x)–top electrode interface to monitor oxygen ion movement during SET and RESET programming cycles in resistive random access memories (RRAMs) (left panel)[93]. The Raman spectrum of graphene shows the corresponding shift in the G-peak position and the amplitude change in the 2D-peak[94] for many SET and RESET cycles, indicating that oxygen ions migrate towards the graphene surface during SET cycles (right panel). **b** | Graphene can serve as a passivation layer with excellent optical properties (approximately 90% transmittance in the visible wavelength range with a sheet resistance as low as ~30 Ω/square) to mitigate undesired surface effects in an RRAM[95]. Transmittance versus wavelength curves are shown for an indium tin oxide (ITO)/graphene/ZnO/ITO transparent RRAM stack (blue line) compared to an RRAM stack without graphene (ITO/ZnO/ITO) (red line). Graphene does not affect the optical properties of the device. **c** | The high-resolution transmission electron micrograph shows an energy-efficient phase-change memory (PCM) cell with graphene as a thermal barrier[23] (left panel), with the top electrode (T.E.), bottom electrode (B.E.) and amorphous $Ge_2Sb_2Te_5$ (a-GST) on a SiO_2 substrate. W plug refers to the heating plug composed of tungsten. Insertion of graphene improves the switching characteristics of the cell, as illustrated by the resistance versus current curves (right panel). The control device (dark blue) in the resistance–current switching curve has a graphene interfacial layer of 1 µm in width, and because of its strong in-plane heat propagation, the RESET-programming current (I_{RESET}) is higher than that in a conventional PCM cell without graphene (pale blue curve). The graphene-inserted PCM (G-PCM) with graphene patterned to be as small as the B.E. heater (red curve) decreases the RESET current by ~40%. **d** | Schematic of a graphene-channel ferroelectric field-effect transistor (FET) (left panel) and corresponding drain current (I_D)–gate voltage (V_G) hysteresis curves (right panel) at different V_G sweep ranges from ± 20 V (bottom curves) to ± 70 V (top curves) for ferroelectric random access memories (fRAMs)[126]. Blue and red curves represent the different voltage sweep directions. The large, tuneable hysteresis (ΔI_D) observed in the graphene/h-BN/PMN-PT device structure is attributed to spontaneous polarization at the ferroelectric material (PMN-PT) surface that controls the electronic structure of graphene. GND, electrical ground. Part **a** is adapted with permission from REF. 93, American Chemical Society. Part **b** is adapted with permission from REF. 95, IEEE. Part **c** is reproduced with permission from REF. 23, American Chemical Society. Part **d** is adapted with permission from REF. 126, American Chemical Society.

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Thermal barriers in PCM

Graphene. Using graphene as a thermal barrier can be exploited to better confine heat within the programming region of a PCM[23] (FIG. 3c). Compared with a conventional PCM cell without graphene, the RESET current decreases ~40% due to the additional thermal resistance of the inserted graphene monolayer[23]. The crucial role of the graphene layer as an effective thermal barrier rather than an additional series resistor is supported by the fact that the RESET current of the graphene-inserted PCM, which has a large area of graphene (1 μm^2) (FIG. 3c), is similar to that of the PCM without graphene. If the graphene layer and its interfaces added series resistance, the RESET current of the large-area-graphene-inserted PCM would be expected to be smaller than that in the PCM without graphene. Furthermore, the low-resistance state (LRS) does not change with the insertion of graphene owing to its minimal electrical contact resistance compared to the resistance of the PCM cell itself. Graphene effectively adds a thermal boundary resistance between the GST alloy and the bottom electrode, as can be described by an analytical model, thereby suppressing the parasitic loss of heat into the electrode[100]. This interfacial thermal engineering technique offers an elegant way to improve the heating efficiency of PCM without substantially altering the cell structure or material.

These results raise the question of whether graphene could be used as a thermal resistor. The function of graphene as a thermal barrier in PCMs[23,100] is somewhat counterintuitive because graphene is known for excellent in-plane thermal conductivity[76]. However, it should be noted that it is the cross-plane thermal conduction that matters. Graphene has a high anisotropy of heat flow: the cross-plane thermal conduction is limited by weak van der Waals interfaces[76,101,102], whereas the in-plane heat transport is facilitated by the strong covalent bonds of sp^2-hybridized carbons. Using a time-domain thermoreflectance (TDTR) technique[23], it has been demonstrated that the inserted graphene layer adds a thermal boundary resistance of 32 ± 10 and 44 ± 3 m^{2}K/GW for graphene interfaces with as-deposited (amorphous) and annealed (fcc-crystalline) GST films, respectively. These thermal boundary resistance values are remarkably high (equivalent to the thermal resistance of a much thicker film of 10–15 nm GST[23]), demonstrating that even a sub-nanometre thin graphene layer can serve as an effective, cross-plane thermal barrier while occupying a negligible volume within an overall PCM bit cell.

Fullerene. The insertion of a semiconducting thin film of C_{60} with low thermal conductivity (~0.4 W (mK)$^{-1}$ at room temperature)[103] to engineer the interface between the phase-change material and the bottom electrode also results in a significant reduction of the RESET current. However, the series resistance added by the 30 nm C_{60} film, which appears as an increase in the on-state (LRS) resistance, might also yield a substantial amount of Joule heating. Future work needs to investigate the role of interfacial heating due to additional electrical resistance to elucidate the potential benefits of the inserted fullerene layer.

Interfacing with ferroelectric material

fRAM relies on ferroelectric materials to form bistable NVM bits through remnant polarizations[35,36]. Conventional ferroelectric materials (for example, $Pb(Zr,Ti)O_3$ (PZT)[104] or $SrBi_2Ta_2O_9$ (SBT)[105]) have been used in combination with metals and semiconductors to create a complete ferroelectric storage system, such as capacitor-based (one transistor and one ferroelectric capacitor (1T1C)) or field-effect transistor (FET)-based (1T) fRAMs[106,107]. In contrast to the capacitor-type fRAM[46,108], the FET-type fRAM can perform read operations non-destructively, thereby offering more reliable and energy-efficient non-volatile data storage.

The discovery of ferroelectricity in HfO_x of the non-centrosymmetric orthorhombic phase[47–52] has revived interest in ferroelectric FET and fRAM; the non-volatile functionality becomes available by use of the HfO_x-based material system that has already been used in CMOS logic technology as a high-k gate insulator[109,110], instead of traditional perovskite ferroelectrics[104,105]. This is an important milestone in ferroelectrics because the practical implementation of the ferroelectric FET on existing CMOS platforms has been a significant challenge owing to the thermodynamic incompatibility of such perovskite oxides with silicon[111], which has made the density scaling of fRAM much slower than that of conventional charge-based semiconductor memories[33,34]. Furthermore, because of the very low conduction band offset between the perovskite oxide and silicon[112,113], thick (a few tens of nanometres) perovskite films and noble-metal electrodes have been required for low-leakage devices[114]. Ferroelectric HfO_x has the potential to enable better process compatibility, device scalability and performance than that of perovskite[47–52], facilitating new ferroelectric FET applications, including fRAM (either stand-alone[115,116] or embedded[117]), 3D ferroelectric NAND[118] and ferroelectric synaptic devices[119].

A key feature of the FET-type fRAM cell is a ferroelectric gate FET with a ferroelectric thin film as the gate dielectric[106,107]. Once the binary data of '0' or '1' are written in the ferroelectric film in the form of opposite directions of polarization, information can be read out as the difference in the drain current of the FET owing to a difference in threshold voltages, which are modulated by the ferroelectric polarization. However, obtaining decent ferroelectric/semiconductor interface quality has proven to be challenging because of interdiffusion or intermixing problems during the crystallization process[106,107]. To overcome these issues, a dielectric buffer layer can be inserted between the Si substrate and the ferroelectric oxide layers at the cost of short data retention owing to the depolarization field[120] and high operation voltages because of the increase in dielectric thickness[106,107]. Introducing ferroelectric HfO_x may help to mitigate these issues because it has a high coercive field (~1 MV cm^{-1}) and a low dielectric constant (which, in turn, leads to a low depolarization field), thus retaining ferroelectricity and obtaining stable NVM functionality even at sub-10 nm thickness[48,52].

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Carbon nanotubes in fRAM. The integration of 1D channels of CNTs on top of ferroelectric thin films to form a ferroelectric gate FET[121] leads to a hysteresis loop owing to the reversible remnant polarization of the ferroelectric material with a large memory window (threshold voltage shift) of approximately 4 V, a long retention time of up to 1 week and ultra-low power consumption on the order of fJ per bit. CNTs have been proposed to be able to form perfect interfaces with ferroelectric oxide materials because of their extremely high chemical stability (no dangling bonds) and mechanical robustness[121]. Multi-bit ferroelectric gate FET memories[122] and double-gate FETs with polymeric ferroelectric films[123] have also been realized, highlighting how carbon nanomaterials have advanced FET-based fRAM technology.

Graphene in fRAM. Graphene has also been integrated into ferroelectric FETs with non-volatile, reversible switching behaviour. In a ferroelectric FET with few-layer graphene integrated as a channel, a resistance hysteresis loop (ΔR/R) of up to ~200% is observed[124], which can be attributed to the electrostatic doping of graphene by electric dipoles at the ferroelectric/graphene interface. Moreover, a variety of emerging ferroelectric crystals have been used as gate dielectrics integrated with a monolayer graphene film to form FETs (for example, $Bi_{3.15}Nd_{0.85}Ti_{2.99}Mn_{0.01}O_{12}$ (BNTM)[125] and (1−x)[$Pb(Mg_{1/3}Nb_{2/3})O_3$]−x[$PbTiO_3$] (PMN-PT)[126]) (FIG. 3d). A transparent, flexible ferroelectric FET built on a polyethylene terephthalate (PET) substrate[127] has also been reported. In contrast to CNT-channel fRAMs[121,122], the performance of graphene-based fRAMs is not yet comparable to that of state-of-the-art ferroelectric FETs built on conventional semiconductors. One issue is that the quality of the ferroelectric/graphene interface needs to be improved. Moreover, the strong substrate dependence of the charge carrier mobility of graphene (for example, unconventional substrates such as hexagonal boron nitride have to be used to ensure high carrier mobility[126]) may limit further commercialization of graphene-channelled fRAM technology because of the increased complexity and fabrication cost of the fRAM substrate preparation.

Memory selectors

For a 2D cross-point resistive-switching memory array, misprogramming or misreading can readily occur because of parasitic conducting (sneak current) paths owing to the wordlines (WLs) and bitlines (BLs) being shared among numerous NVM cells[128]. Integration of a selection device into the memory cell can solve the sneak path problem[22,65], which is a key requirement for the development of 2D and 3D cross-point NVM arrays unless the memory cell itself has self-rectifying or highly nonlinear current–voltage (I–V) characteristics. NVM array architectures have greatly benefited from the use of carbon nanomaterials and nanodevices. Both RRAMs and PCMs are currently being explored for large-scale NVM array technology, which has been accelerated by innovations in carbon nanotube FETs (CNFETs) that can be integrated as memory selectors.

Carbon nanotube FETs

The first CNT-based memory selector was based on high-performance CNFETs that were tightly integrated with PCM bit cells[129]. The cells can be selectively programmed in a 1-transistor-n-resistors (1TnR) configuration by turning the back-gated CNT transistor, which is formed by the semiconducting CNT channel, on and off (FIG. 4a). The use of a 1D selector limits the sneak leakage currents within the selected CNT wordline for RRAM or PCM cells that are integrated in the crossbar array[130] (FIG. 4b).

CNFET selectors fulfil several requirements of an ideal selector for a high-density RRAM crossbar array. The high ON/OFF ratio (I_{ON}/I_{OFF} >10^6) enables high selectivity of memory bits, the ultra-low OFF-state leakage current (I_{OFF} <10 pA) accommodates unselected and half-selected cells in large-scale arrays, and the high on-state current density (J_{ON} >10 MA cm^{-2}) makes it possible to programme nanoscale NVM bit cells. The low-processing temperature (<300 °C) facilitates 3D stacking, and bipolar operation (nearly symmetric I–V characteristics) enables best-of-breed RRAM operation[130]. The CNFET selection device can be tightly integrated with n resistive-switching elements (1TnR configuration) without requiring an increased area footprint, offering a practical engineering methodology for trade-off between device density and array performance (for example, write voltage margin)[129,130]. By contrast, Crossbar Inc. developed a crossbar RRAM array[131] by using an access transistor (1T, not serving as a selector) outside the active memory array to manage a large number of interconnected RRAM cells (nR); this configuration still requires additional selection devices to be integrated at each cross-point of WLs and BLs[132].

Resistive-switching media

The integration of electronics for non-planar and malleable platforms is required for flexible electronics. Carbon nanomaterials such as graphene oxide (GO) and other composite materials have advanced low-cost, flexible nanoelectronics by providing a thin and flexible resistive-switching material for memory.

Carbon nanomaterials for flexible RRAM

GO is a graphene sheet with attached oxy functional groups, such as epoxide, hydroxyl and carboxyl groups[133]. The chemically reduced form, reduced GO (rGO), has been used to produce graphene in large quantities[134]. GO and rGO are flexible and stretchable, are easily fabricated through solution processing and have beneficial electrical, thermal, mechanical and optical properties (TABLE 1). Therefore, these two materials have been used for the development of devices such as pressure sensors[135], thermal rectifiers[136] and light emitters[137]. In particular, GO and rGO have enabled the fabrication of flexible RRAM devices by providing a resistive-switching medium that is readily accessible by and can be integrated with flexible surfaces and substrates.

GO thin films sandwiched between conventional metal electrodes (Cu and Pt) show resistive-switching characteristics with switching voltages of <1 V, a retention

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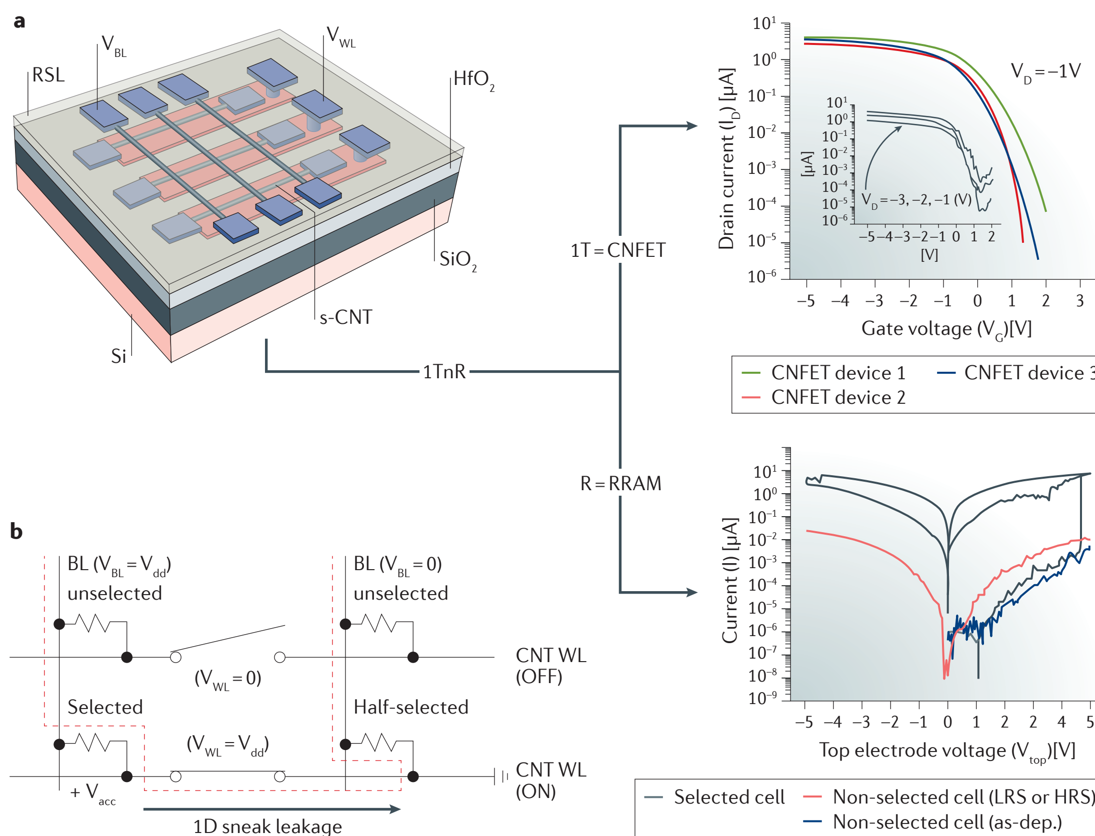

Figure 4 | **Carbon nanotube field-effect transistors for high-density non-volatile memory crossbar arrays.** **a** | Schematic of a one-transistor-n-resistors (1TnR) non-volatile memory (NVM) array architecture with semiconducting carbon nanotubes (s-CNTs) integrated as wordlines[130]. V_{BL} and V_{WL} represent voltages applied to the bitline (BL) and wordline (WL), respectively[66]. The back-gated carbon nanotube field-effect transistors (CNFETs) serve as 1D selectors for resistive-switching layers (RSLs). RSLs can be either metal oxides for resistive random access memories (RRAMs) or phase-change alloys for phase-change memories (PCMs). The two right-hand panels show the I_D–V_G curves for the CNFET (top) and the current (I)–V_{top} curves for an RRAM integrated with CNFETs (bottom). Top panel: the I_D–V_G characteristics at a drain voltage (V_D) of −1 V are shown for three CNFET devices (red, blue and green). The ultra-low OFF-state leakage currents (I_{OFF}) of <10 pA along with very high ON/OFF current ratios of 10^5–10^6 suggest that with an applied gate voltage of ~2 V, the unselected cells (that is, the memory cells on the CNT wordlines that are not selected[66]) would pass extremely small sneak leakage currents. The half-selected cell (that is, the memory cell on the selected wordline but on the unselected bitline[66]) experiences a larger voltage drop in the crossbar NVM array. The inset shows that even though V_D is more negative (that is, changes from −1 V to −3 V), I_{OFF} of the CNFET remains at ~1 nA for V_D = −3 V, which indicates that the currents through the half-selected cell are negligible. Bottom panel: only selected AlO_x cells experience resistive-switching in the 1TnR array (forming at approximately 4.5 V, RESET at approximately −4.5 V and SET at approximately 3 V) because the integrated CNFET selector is fully turned on with a V_{WL} of −5 V. The other non-selected cells (red and blue curves) are on the same CNFET but with a positive gate voltage of +2 V. Unlike in the selected cell case, the turned-off CNFET is highly resistive and can carry only a small amount of current (not sufficient to induce resistive-switching). **b** | Illustration of 1D sneak leakage confined in the 1D CNT channel in a 1TnR configuration[130]. The write access voltage (V_{acc}) across the selected memory cell (bottom left corner) highlights that a voltage as large as the supply voltage (V_{dd}) can be induced at the selected cell owing to a reduction in sneak path leakages through the use of CNFETs (2D leakage currents across WLs are blocked because of the high resistances of non-selected (turned-off) CNT WLs). as-dep., as deposited; HRS, high-resistance state; LRS, low-resistance state. Parts **a** and **b** are adapted with permission from REF. 130, IEEE.

time of 10^4 seconds and programming endurance of 100 cycles[138] (FIG. 5a). Based on these characteristics, GO-based RRAMs, which are integrated with flexible electrodes (such as Al) and substrates (such as polyethersulfone)[139], have been developed. Thermally reduced GO films in such RRAMs can reach R_{OFF}/R_{ON} ratios of >100 and endurance cycles of approximately 250 (REF. 140) (FIG. 5b). However, the performance of GO-based and rGO-based RRAMs is still worse than that of state-of-the-art metal-oxide-based RRAMs (FIG. 5c). Further studies are required to better understand the resistive-switching and failure mechanisms of these GO-based and rGO-based RRAM devices[141].

Alternatively, carbon nanomaterials can be embedded in a polymeric matrix to provide the resistive-switching medium of organic RRAM cells. For example,

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a composite film of poly(*N*-vinylcarbazole) (PVK) and C_{60}, sandwiched between Al and ITO electrode layers[142], shows bipolar switching behaviour (FIG. 5d) and can act as non-volatile storage with R_{OFF}/R_{ON} ratios of more than 10^5. This behaviour can be attributed to the electric-field-induced charge transfer from the carbazole (electron donor) to the C_{60} (electron acceptor)[142]. Other carbon nanomaterials, such as the C_{60} derivative phenyl-C61-butyric acid methyl ester (PCBM)[62], CNTs[143,144], graphene[145] and functionalized GOs[146], have also been explored for the development of polymer–carbon composite-based RRAMs, providing a promising

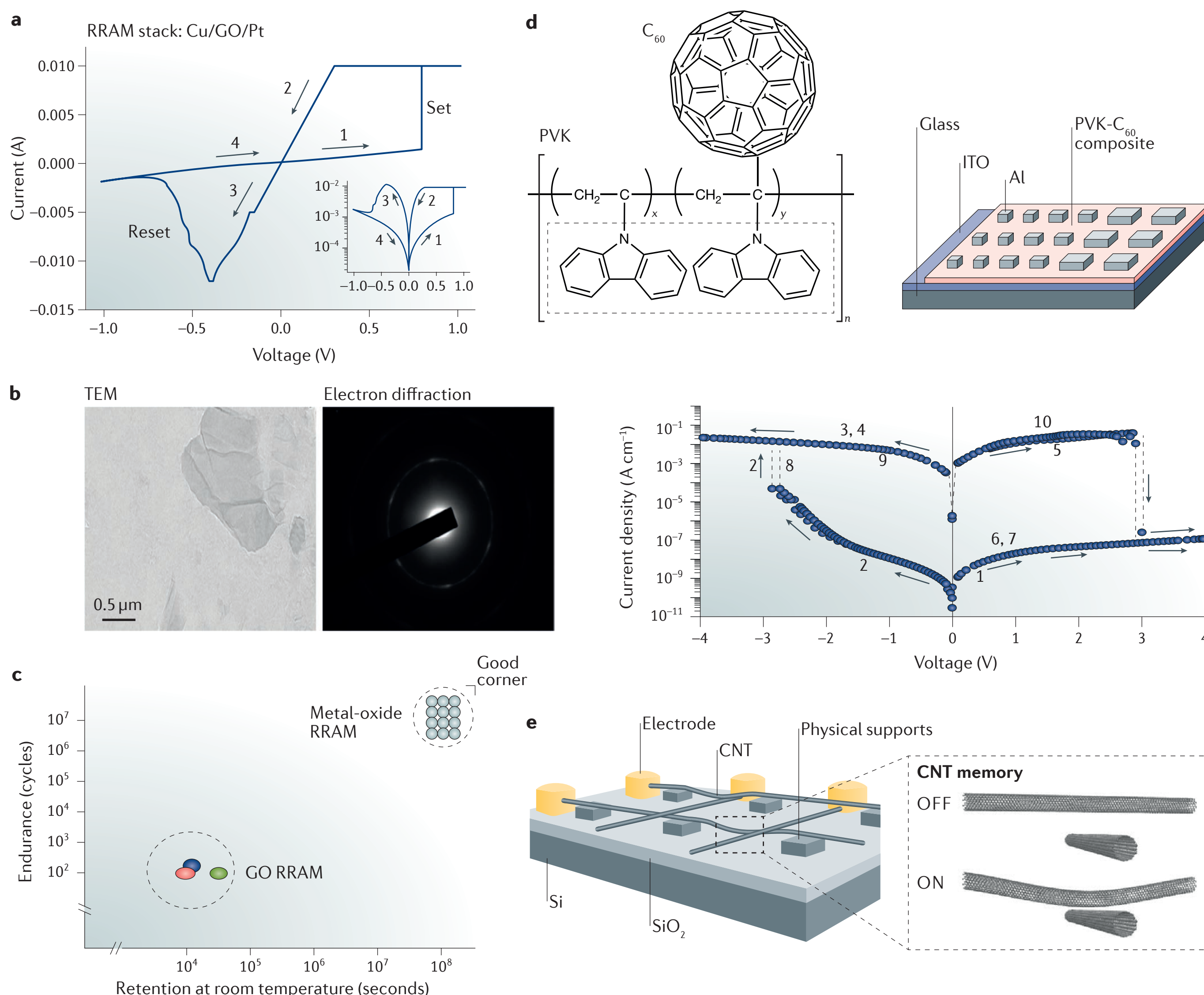

Figure 5 | **Graphene oxide and other carbon-based composites. a** | Current (I)–voltage (V) curve for a Cu/graphene oxide (GO)/Pt resistive random access memory (RRAM) stack showing non-volatile resistive-switching behaviour (inset: I–V in log scale)[138]. The carbon nanomaterial itself (GO[138,139] or reduced GO (rGO)[140]) can exhibit memristive switching behaviour that resembles that of a conventional metal-oxide-based RRAM. **b** | Transmission electron micrograph (TEM) and corresponding electron diffraction pattern of thermally reduced GO films[140]. **c** | Endurance and retention characteristics of GO-based and rGO-based RRAMs[138–140] compared with state-of-the-art metal-oxide-based RRAMs[19]. Further studies are required to develop GO (or rGO) RRAM with better reliability (endurance and retention) characteristics (towards the good corner in the figure). **d** | The polymeric composite of poly(*N*-vinylcarbazole) (PVK) and fullerene (C_{60}) can be integrated as a resistive-switching medium with flexible electrodes (Al and indium tin oxide (ITO)), featuring a high ON/OFF resistance ratio as illustrated in the current density–voltage curve[142]. The sweep sequence and direction are indicated by the number and arrow, respectively (the fourth and seventh sweeps are conducted after the power is turned off). **e** | Schematic of a carbon nanotube (CNT)-based memory device based on suspended CNT device architecture[152]. Bi-stable non-volatile memory bits could be achieved through the contacted (ON) or separated (OFF) nanotubes. Part **a** is adapted with permission from REF. 138, American Institute of Physics. Part **b** is adapted from REF. 140, Macmillan Publishers Limited. Part **d** is adapted with permission from REF. 142, American Chemical Society. Part **e** is adapted with permission from REF. 152, AAAS.

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alternative to conventional inorganic semiconductor-based memory technologies by potentially enabling applications such as wearable electronics, smart watches, glasses, fabrics[147] and epidermal electronic systems[148,149].

Carbon nanotube memory

Carbon nanotube memory is a generic term for NVMs using CNTs as a storage layer. The switching behaviour (for example, I–V characteristics) of the CNT storage layer is not necessarily equivalent to that of metal-oxide-based RRAM. However, CNT memory can be considered to be an RRAM because the information readout is based on a reversible resistance change. CNT memory has been based on the hysteresis loop of the I–V characteristics of CNTs (I_D (drain current) versus V_D (drain voltage)[150] or I_D versus V_G (gate voltage)[151]) or on the electromechanical change of the CNT arrangement[152]. For example, semiconducting CNTs generate a reproducible I–V hysteresis curve in a two-terminal geometry without a third terminal (gate)[150] owing to charge trapping at the CNT/dielectric interface. Despite a limited reliability of only 10^3 endurance cycles, this two-terminal, CNT-based NVM device can be constructed with high R_{OFF}/R_{ON} ratios of more than 10^4. A transparent, flexible CNT memory using oxygen-decorated graphene as electrodes[151] has also been developed based on the hysteretic I_D–V_G curve of CNTs. This transparent device consumes very low operating currents of around or below 1 nA and shows remarkable 10^3 cycles bending strength. Alternatively, NVM bits could be realized by inducing an electromechanical change in CNTs[152]. Although its working principle is not yet clearly understood, Nantero's NRAM, which reportedly will soon be commercialized, represents a similar CNT memory technology relying on the electromechanical properties of CNTs[153] (FIG. 5e).

Conclusions

NVM technologies are rapidly advancing. The solid-state drive (SSD) product Optane, which was developed and recently released by Intel and Micron[154], represents the first 3D cross-point memory technology and has thus opened new opportunities to optimize the memory hierarchy[155]. Carbon nanomaterials are playing an important role in the development of low-power, high-density and reliable NVMs (FIG. 6). However, there are still major challenges to address in terms of the manufacturing, integration, mechanism and specific material properties to foster the use of carbon nanomaterials for NVM technology.

Manufacturing and integration

Although the physical size and the electrical and thermal properties of carbon nanomaterials make them ideal candidates for applications in nanoelectronics, challenges in manufacturing limit their integration into high-density NVM arrays. One key challenge is the controlled growth or synthesis of high-quality carbon nanomaterials. Different strategies have been proposed to obtain high-quality graphene films, for example, including exfoliation from natural or non-natural sources of graphite[156], growing graphene on SiC single crystals[157] and chemical vapour deposition (CVD) to grow graphene on metal[158,159] or insulating[160] substrates. Exfoliated graphene is of high quality in terms of carrier transport properties, but large-scale integration and manufacturing remain challenging. The area of graphene flakes is currently limited to only hundreds of square micrometres. Graphene films grown on SiC substrates are also restricted by substrate size. By contrast, using CVD, graphene growth is limited only by the deposition chamber itself[77]. Therefore, CVD, which typically relies on a catalytic reaction between a carbon precursor (for example, methane or ethylene) and a metal substrate such as copper, enables the growth of a single layer of graphene on large metal substrates[158]. Furthermore, the quality of the CVD graphene film is nearly equivalent to that of graphene exfoliated from natural graphite[161,162].

The most important hurdle to using low-dimensional nanostructures for NVM device applications is the transfer process. The high temperature (~1,000 °C) required for the CVD process is incompatible with existing CMOS platforms. Thus, a dry or wet process is typically required to transfer nanomaterials from the metal onto the device substrate. This transfer process can lead to the exposure of the material surface to organic and/or inorganic contaminants[158,163–165]; therefore, it is important to maintain the as-grown surface and carrier transport properties of the nanomaterial[23] and to prevent physical damage caused by the subsequent microfabrication process[130]. For example, in graphene-inserted PCM[23], the electrical contact resistance of graphene can be minimized by keeping the physical support layer made of poly(methyl methacrylate) (PMMA) fresh before transfer and optimizing the conditions for PMMA removal after transfer. Other post-transfer approaches, including mechanical cleaning[166], thermal annealing, wet chemical treatment[167] and plasma cleaning[168], may be implemented to further reduce contamination of the carbon nanomaterial surface.

Passive versus active electrodes

Carbon-based electrodes can simply serve as a type of small electrode (passive) or they can directly contribute to NVM operation (active). In RRAMs, CNTs[73,75] and graphene films[169] have been extensively studied as passive electrodes for the development of nanoscale memory bit cells and the investigation of the fundamental scaling limit. However, carbon nanomaterials could also serve as active electrodes participating in the memory operation beyond the down-scaling of the cell size. For example, in a 3D vertical RRAM with graphene edge electrodes[82], the graphene monolayer functions as an atomically thin oxygen reservoir. Oxygen ions migrate between the graphene reservoir and the adjacent metal-oxide sidewall layer during SET and RESET operations (FIG. 2a). Additionally, compared with a conventional metal electrode, the use of graphene electrodes leads to a smaller tail-end thickness of the conductive filament at the graphene edge/metal-oxide interface and thus to higher cell resistances in the HRS and consequently lower SET-compliance currents. Using carbon

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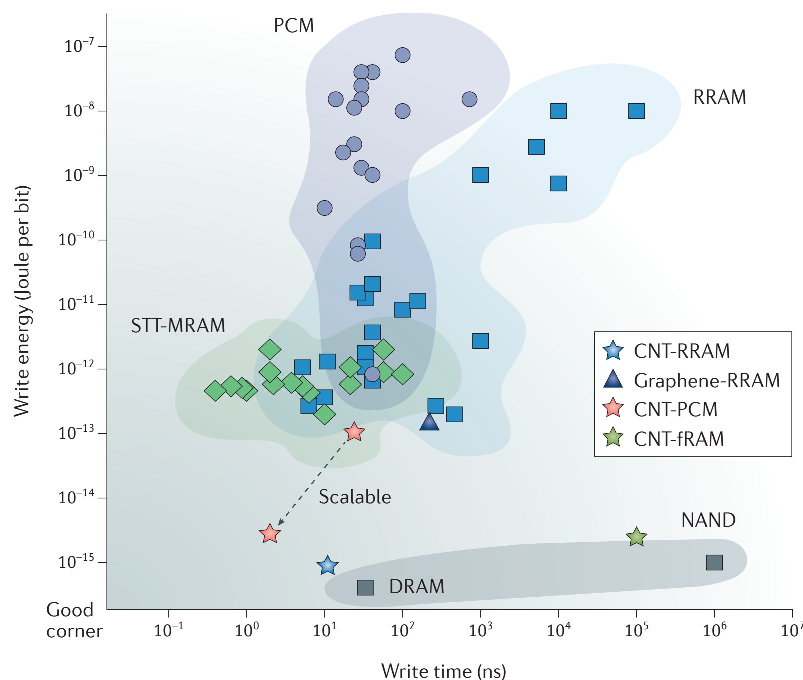

Figure 6 | **Ashby plot for non-volatile memories.** The Ashby plot compares carbon nanomaterial-based non-volatile memories (NVMs), carbon nanotube resistive random access memory (CNT-RRAM), graphene-RRAM, CNT-phase-change memory (CNT-PCM) and CNT-ferroelectric random access memory (CNT-fRAM), with conventional NVMs (PCM, RRAM, spin-transfer-torque magnetic RAM (STT-MRAM)) without carbon nanomaterials, showing the write energy of the memory cell (Joule per bit) and write time (nanoseconds). Small write energy and write time are considered as a good corner. The data for state-of-the-art STT-MRAM, PCM and RRAM without carbon nanomaterials have been collected from the Stanford Memory Trend[58]. The performances of contemporary memory (such as DRAM) and storage (such as NAND) devices are also compared in the figure. The CNT-crossbar RRAM[74] has a write energy on the order of fJ, similar to that of DRAM or NAND, while operating at a faster switching speed of 10 ns. The RRAM with graphene as atomically thin edge electrodes represents a high-density, bit-cost scalable 3D NVM array architecture with an energy consumption comparable to the lowest known values of conventional RRAMs[82]. The PCM device using CNT electrodes operates with a 20 ns pulse and an energy consumption of approximately 100 fJ. However, the write energy of CNT-based PCMs could be further scaled down to single fJ per bit by reducing the memory bit size[59,85]. Despite the potential of fRAM to operate with speeds faster than that of NAND and comparable to that of DRAM, the experimental demonstration of CNT-enabled fRAM devices has been limited to 100 µs pulse width (switching speed), while achieving a very low energy consumption on the order of fJ (REF. 121).

nanomaterials as active memory electrodes certainly has great potential to modulate the operational principle and thus the switching behaviour of NVMs[82]. Future research needs to investigate the fundamental physical mechanism of how carbon nanomaterials enable the unique NVM device characteristics (for example, the very-low-power operational mode of graphene-inserted 3D vertical RRAM[82]).

Specific material requirements

Certain NVM technologies demand specific material properties. For example, PCM requires the resistive-switching medium to switch between the crystalline and amorphous phase through Joule heating, which is not easily achievable with carbon-based materials owing to their high phase-transition temperatures. For example, the conversion of amorphous carbon wires into sp^2-hybridized crystalline structures through Joule heating occurs above 2,000 °C (REFS 170,171); therefore, the use of carbon nanomaterials for PCM is limited to electrodes, interfacial engineering layers and selectors. STT-MRAM technology stores information in ferromagnetic metal electrodes. Ferromagnetism is determined by the electrons in the *d* and *f* orbitals, which carbon atoms do not have. Pristine graphene is a strong diamagnetic material, but the formation of magnetic moments in carbon nanomaterials is not trivial. Despite theoretical and experimental approaches to introduce dopants and adatoms into graphene[172,173], the induction of magnetic moments in carbon-based nanomaterials suitable for NVM application has not yet been achieved. Future studies investigating the possibility of altering the magnetic properties of carbon nanomaterials may contribute to the advancement of STT-MRAM technology and spintronics.

Other monoatomic low-dimensional materials

Carbon has been the most successful material to be transformed into various low-dimensional nanostructures, such as C_{60} (0D), CNTs (1D) and graphene (2D), and these materials have contributed to advances in a variety of applications, including NVMs. However, there are other materials capable of forming certain low-dimensional structures. 2D atomic sheets[174], such as semiconducting transition metal dichalcogenides[175], and monoatomic crystals termed Xenes have emerged as candidates for low-dimensional materials for flexible nanoelectronics[176]. Xenes, including silicene[177], germanene[174] and phosphorene[178], are of great interest in the field of nanoelectronics. However, many basic questions remain to be experimentally and theoretically addressed. Sustained research efforts investigating current challenges, such as air stability, interface quality and device integration, will potentially pave the way for the post-silicon electronics era.

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