Gate tunneling current and quantum capacitance in metal-oxide-semiconductor devices with graphene gate electrodes

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Metal-oxide-semiconductor (MOS) devices with graphene as the metal gate electrode, silicon dioxide with thicknesses ranging from 5 to 20 nm as the dielectric, and *p*-type silicon as the semiconductor are fabricated and characterized. It is found that Fowler-Nordheim (F-N) tunneling dominates the gate tunneling current in these devices for oxide thicknesses of 10 nm and larger, whereas for devices with 5 nm oxide, direct tunneling starts to play a role in determining the total gate current. Furthermore, the temperature dependences of the F-N tunneling current for the 10 nm devices are characterized in the temperature range 77–300 K. The F-N coefficients and the effective tunneling barrier height are extracted as a function of temperature. It is found that the effective barrier height decreases with increasing temperature, which is in agreement with the results previously reported for conventional MOS devices with polysilicon or metal gate electrodes. In addition, high frequency capacitance-voltage measurements of these MOS devices are performed, which depict a local capacitance minimum under accumulation for thin oxides. By analyzing the data using numerical calculations based on the modified density of states of graphene in the presence of charged impurities, it is shown that this local minimum is due to the contribution of the quantum capacitance of graphene. Finally, the workfunction of the graphene gate electrode is extracted by determining the flat-band voltage as a function of oxide thickness. These results show that graphene is a promising candidate as the gate electrode in metal-oxide-semiconductor devices. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4968824]

There has been a significant research interest in graphene for electronic applications, due to its good electrical conductivity, high optical transparency, mechanical flexibility, thermal stability, and two-dimensional structure.[1,2] The potential of graphene as a planar channel material replacing silicon in digital logic circuits, however, is limited due to the absence of a bandgap. On the other hand, graphene is an excellent candidate for the next generation transparent, conductive, and flexible electrodes for applications such as touch screens, electronic paper, light-emitting diodes, solar cells, gas sensors, and photodetectors.[1–11]

Graphene is also a promising candidate as the gate electrode in metal-oxide-semiconductor (MOS) devices,[12,13] particularly when transparency or workfunction tunability is a requirement. Unlike conventional metals, whose Fermi level is typically pinned at the surface, the Fermi level and hence workfunction of graphene can be tailored by electrostatic gating,[14–16] chemical or contact doping,[17,18] surface engineering,[19] or varying the number of graphene layers.[13,20] As a result, graphene could be utilized as the gate electrode for both NMOS and PMOS devices.[20,21] Furthermore, due to its transparent nature, graphene could also be used as the gate electrode in transparent gate MOS transistors for photodetector and sensing applications.[22]

In a recent study, graphene has been used as the gate electrode of a nonvolatile charge-trap flash (CTF) memory device to replace TaN metal on top of a high-κ dielectric.[12] In another recent study, multi-layer graphene was incorporated between TiN metal gate and SiO_2 in an MOS capacitor structure.[23] In both cases, it was shown that graphene electrodes improve the device performance. Although these few recent studies indicate that graphene holds promise as a gate electrode in MOS devices, a detailed study of the electrical properties of graphene/SiO_2/Si MOS structures is currently lacking, in particular, the study of the gate tunneling current and the effect of the graphene quantum capacitance. A detailed investigation of MOS devices with graphene acting as the metal gate electrode would be of great importance for assessing the potential of integrating graphene into silicon technology.

In this paper, we experimentally fabricate and characterize the MOS devices with chemical vapor deposition (CVD) grown monolayer graphene as the metal electrode, silicon dioxide with thicknesses ranging from 5 to 20 nm as the dielectric, and *p*-type silicon as the semiconductor. We first demonstrate that Fowler-Nordheim (F-N) tunneling dominates the gate current in these devices for oxide thicknesses of 10 nm and higher, whereas for devices with 5 nm oxide, direct tunneling starts to play a role in determining the total gate current. We also characterize the temperature dependence of the F-N tunneling in these devices in the

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range 77–300 K. We extract the F-N coefficients, as well as the effective tunneling barrier height, as a function of temperature. In addition, we perform capacitance-voltage (*C-V*) measurements on these MOS devices and observe a local capacitance minimum under accumulation for thin oxides. By analyzing the data using numerical calculations, we show that this is due to the contribution of the quantum capacitance of graphene, resulting from its low density of states (DOS). Finally, we extract the workfunction of graphene from the *C-V* measurements[24] at various oxide thicknesses. Our results provide fundamental information on the electronic properties of MOS devices with graphene gate electrodes, which is important for the heterogeneous integration of graphene into silicon technology.

We fabricated MOS devices with four different oxide thicknesses along with a control device with no intentional oxide, as explained in detail in the supplementary material and shown in Fig. 1.

Figure 2(a) shows the room temperature *I-V* characteristics of the graphene/SiO_2/Si MOS devices with four different oxide thicknesses ranging from 5 nm to 20 nm, as well as the *I-V* characteristics of the control device with no intentional oxide between graphene and Si, all under negative gate bias. The control device behaves as a metal-semiconductor (MS) Schottky junction.[10,11] It can be seen from Fig. 2(a) that the *I-V* characteristics of the MOS devices exhibit exponential behavior as a function of gate voltage at a fixed oxide thickness and the current level decreases with increasing oxide thickness at a fixed gate voltage. Furthermore, the magnitudes at a fixed gate voltage and slopes of the gate currents

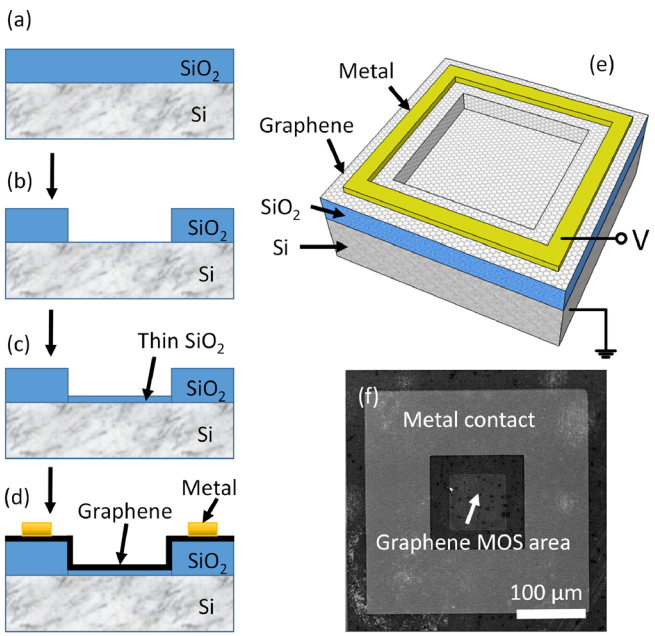

FIG. 1. Schematic of the fabrication process flow for the graphene/SiO_2/Si MOS devices: (a) 300 nm field oxide is thermally grown on *p*-type silicon substrates, (b) active area windows are opened in the field oxide by photolithography and buffered oxide etch (BOE), (c) a thin gate oxide layer with a thickness of 5, 10, 15, or 20 nm is thermally grown in the active area windows, (d) graphene, which is grown by CVD on copper foil, is deposited and patterned on the Si/SiO_2 substrate, and Ti/Au metal contacts are patterned over the graphene on the field oxide. (e) Three-dimensional schematic illustration of the graphene/SiO_2/Si MOS device showing the final structure. (f) Top-view scanning electron microscope (SEM) image of a fabricated MOS device.

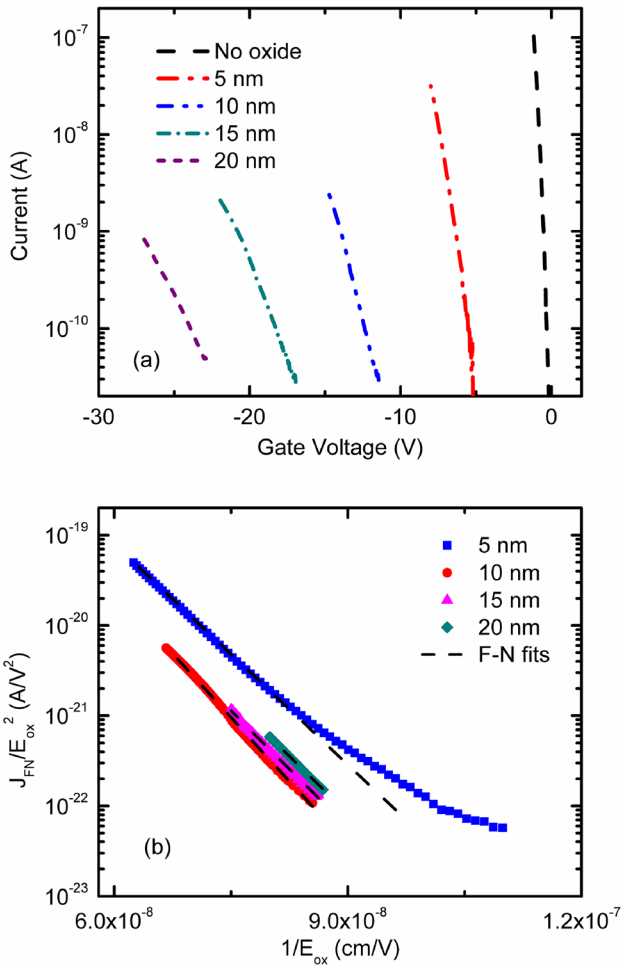

FIG. 2. (a) Room temperature current-gate voltage (*I-V*) characteristics of four graphene/SiO_2/Si MOS devices with different oxide thicknesses and a control device with no intentional oxide between graphene and Si, as labeled. (b) Fowler-Nordheim plots of the four MOS devices with different oxide thicknesses shown in part (a). The F-N plots can be fit by straight lines, as shown by the dashed lines, except for the MOS device with 5 nm oxide, which begins to deviate from a straight line fit at low electric fields due to the contribution of direct tunneling.

of MOS devices are significantly smaller than those of the graphene/silicon Schottky junction control device. This suggests that, in contrast to the control device where thermionic emission over the Schottky barrier dominates the electronic transport,[10,11] tunneling current dominates the electronic transport in the MOS devices.[25]

Fowler-Nordheim (F-N) tunneling describes the tunneling of electrons through a triangular potential barrier, which results in a current I_{FN} given by[25–28]

$$I_{FN} = A_G A E_{ox}^2 \exp\left(-B/E_{ox}\right), \tag{1}$$

where A_G is the device area, E_{ox} is the electric field in the oxide, and A and B are the pre-exponential and exponential F-N coefficients, respectively, defined as[26]

$$A = q^3(m/m_{ox})/8\pi h\Phi_b \quad \text{and} \tag{2}$$

$$B = 8\pi\sqrt{2m_{ox}\Phi_b^3}/3qh, \tag{3}$$

where q is the electron charge, m is the free electron mass, m_{ox} is the effective electron mass in the oxide, h is the

Planck constant, and Φ_b is the effective barrier height given in the units of eV. The plot of $\ln(J_{FN}/E_{ox}^2)$ vs. $1/E_{ox}$, where $J_{FN} = I_{FN}/A_G$ is the current density, is known as the F-N plot and yields a straight line if the transport through the MOS device is Fowler-Nordheim tunneling. The coefficients A and B can be extracted from the y-intercept and slope of the F-N plot, respectively.

Figure 2(b) shows the F-N plots of the four MOS devices with oxide thicknesses ranging from 5 to 20 nm, obtained from the data in Fig. 2(a). Since the applied gate voltage is negative, the F-N current is due to the tunneling of electrons from the graphene gate electrode into the oxide conduction band and the p-type silicon substrate is under accumulation. F-N tunneling of holes from the valence band of silicon into the valence band of oxide could be neglected due to a hole barrier height that is almost 1.5 eV higher. The F-N plots of MOS devices with 10, 15, and 20 nm oxide can be fit by a straight line, as shown in Fig. 2(b), suggesting that Fowler-Nordheim tunneling is the dominant electronic transport mechanism for oxide thicknesses greater than or equal to 10 nm. The MOS device with 5 nm oxide, on the other hand, begins to deviate from a straight line fit at low electric fields, as shown in Fig. 2(b). This indicates that direct tunneling starts to play a role in determining the total gate current, which is the sum of the F-N and direct tunneling components.[26,28] In the direct tunneling regime, there could also be a contribution from the direct tunneling of holes. In addition to direct tunneling, trap-assisted tunneling could also contribute to the total tunneling current for the 5 nm oxide device at low gate voltages. Stress induced leakage current measurements would need to be performed to elucidate any contributions from trap-assisted tunneling.

For obtaining the F-N plots, the electric field in the oxide E_{ox} can be calculated by $E_{ox} = (V_g - V_{FB} - V_S - \Delta V_{ch})/t_{ox}$, where V_g is the gate voltage, V_{FB} is the flat band voltage, V_s is the voltage drop across silicon (i.e., silicon surface potential) under accumulation, ΔV_{ch} is the change in the graphene electrostatic potential with gate voltage due to the Fermi level shift in graphene, and t_{ox} is the oxide thickness.[29,30] For the measurements in this study, the gate voltage V_g is much larger than V_{FB}, V_S, and ΔV_{ch}, and E_{ox} can be approximated as $E_{ox} \approx V_g/t_{ox}$.[27,29,31] This approximation induces an error of as high as 10% in the E_{ox} calculation at the lowest V_g magnitudes for the 5 nm thick oxide. For thicker oxides, the approximation is significantly better since the magnitudes of V_g are much larger. Furthermore, it can be seen from Fig. 2(b) that the F-N plot for the 5 nm oxide device exhibits a higher normalized current density magnitude compared to the plots of other oxide thicknesses. The approximation in the E_{ox} calculation and the contribution of direct tunneling could be the main contributors to this higher current density.

In order to investigate the temperature dependence of the F-N gate tunneling current in the graphene/SiO_2/Si MOS devices, we also performed I-V characterization of the 10 nm oxide device at various temperatures ranging from 77 K to 300 K. Figure 3(a) shows the F–N plots of this device at eight different temperatures. As we can see from the best fits in the figure, the F-N plots remain linear at all temperatures, whereas their slopes decrease as temperature increases from 77 K to 300 K. The good linearity of the F-N plots indicates

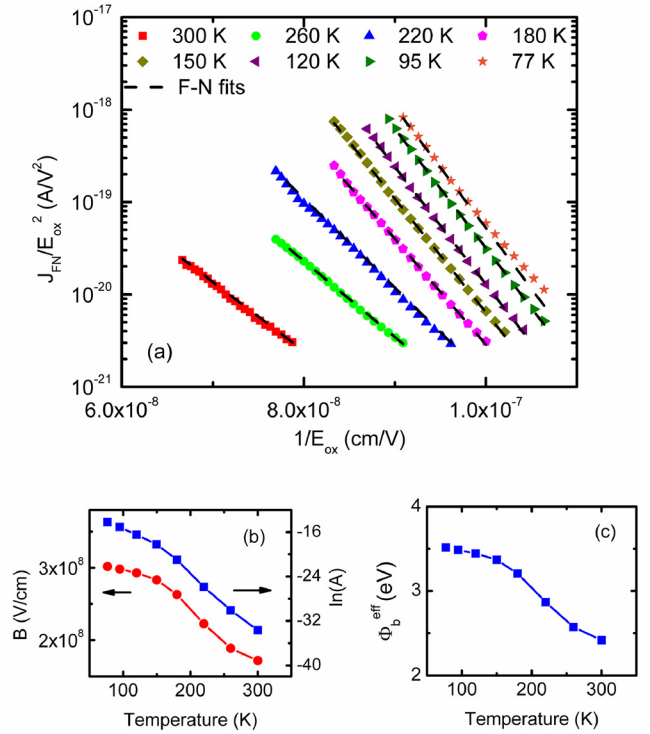

FIG. 3. (a) Fowler-Nordheim plots for a graphene/SiO_2/Si MOS device with 10 nm oxide at eight different temperatures ranging from 77 K to 300 K. The linear F-N fits are shown by the dashed lines. (b) F-N coefficients ln(A) (blue squares, right y-axis) and B (red circles, left y-axis) as a function of temperature, extracted from the F-N fits shown in part (a). (c) The effective barrier height Φ_b^{eff} as a function of temperature, calculated from the extracted values of B shown in part (b).

that, although Eq. (1) is derived under the low temperature approximation, it can still be used to empirically describe the F-N current at all temperatures with temperature dependent *effective* F-N coefficients $A(T)$ and $B(T)$.[30,32]

Figure 3(b) shows the F-N coefficients ln(A) (right y-axis) and B (left y-axis) as a function of temperature, extracted from the F-N fits to the data shown in Fig. 3(a). It is evident from the figure that both ln(A) and B decrease with increasing temperature. Figure 3(c) shows the values of the effective barrier height Φ_b^{eff} as a function of temperature, calculated from the extracted values of B by re-arranging Eq. (3) as $\Phi_b^{eff}(T) = (3qhB(T)/(8\pi\sqrt{2m_{ox}}))^{2/3}$. We have extracted $\Phi_b^{eff}(T)$ from $B(T)$ as commonly done, since this is more reliable compared to extraction from $A(T)$, as discussed in the literature.[30,32] Here, we assumed a temperature independent effective mass of $m_{ox} = 0.5\,m$.[30,32,33] It can be seen from the figure that Φ_b^{eff} decreases from ~3.5 eV to 2.5 eV as temperature increases from 77 to 300 K. This decrease in Φ_b^{eff} with increasing temperature agrees with the trend observed in the previous experiments on the temperature dependence of the F-N current in conventional MOS devices with polysilicon or metal gate electrodes.[27,30,32,34–38]

In addition to the gate leakage current, the gate capacitance is one of the most important parameters of an MOS device. We also performed high-frequency C-V measurements on the graphene/SiO_2/Si MOS devices with different oxide thicknesses at a frequency of 100 kHz, as shown in Fig. 4(a). It is clear from this figure that, in contrast to conventional

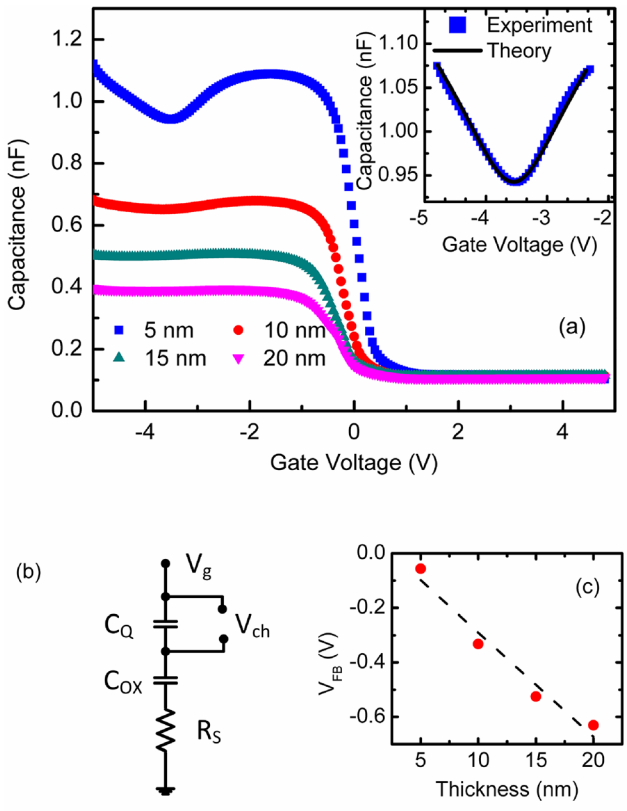

FIG. 4. (a) High frequency (100 kHz) *C-V* characteristics at room temperature of four graphene/SiO_2/Si MOS devices with oxide thicknesses ranging from 5 to 20 nm. The inset shows the zoom-in of the experimental capacitance dip observed under accumulation for the 5 nm oxide device, as well as the theoretical best-fit based on the quantum capacitance of graphene in the presence of potential fluctuations induced by charged impurities. (b) Small-signal equivalent circuit diagram of the graphene/SiO_2/Si MOS device under accumulation, showing the quantum capacitance of graphene C_Q, the oxide capacitance C_{ox}, and the series resistance R_s in series. (c) The flat-band voltage, extracted from the *C-V* curves as a function of oxide thickness, for the devices in part (a). The dashed line shows the linear best fit of the extracted data.

high-frequency MOS *C-V* characteristics,[25,26] a capacitance dip under accumulation (negative V_g) is observed for thin oxides, most notably for the 5 nm oxide device. This local minimum in the *C-V* data under accumulation is due to the contribution of the quantum capacitance of graphene.[39–46] The oxide capacitance per area C_{ox}, given by $C_{ox} = \varepsilon_{ox}/t_{ox}$, where ε_{ox} is the permittivity of oxide and t_{ox} is the oxide thickness, and the quantum capacitance of graphene per area C_Q are in series, as shown in the small-signal equivalent circuit diagram of Fig. 4(b). Therefore, the contribution from the quantum capacitance of graphene is observable only for thin oxides, where C_{ox} is large. C_Q is given by[45–47]

$$C_Q(V_{ch}) = \frac{\partial Q}{\partial V_{ch}} = q^2 \int_{-\infty}^{\infty} D_{gr}(E)\left(-\frac{\partial f(E,E_F)}{\partial E}\right)dE, \quad (4)$$

where Q is the net charge per area in the graphene sheet, V_{ch} is the graphene electrostatic potential given by $V_{ch} = -E_F/q$, where E_F is the graphene Fermi level (chemical potential), $D_{gr}(E)$ is the density of states (DOS) of graphene per unit area, and $f(E,E_F)$ is the Fermi-Dirac distribution function. The reference of energy and potential is taken as the Dirac point. It is evident from Eq. (4) that the effect of quantum capacitance can only be observed for gate electrode materials having a low density of states, such as graphene, leading to a small C_Q relative to C_{ox}.

It has been well established that charged impurities lead to electron-hole puddles and cause random local electrostatic potential fluctuations in real graphene sheets.[10,43,46,48–50] These potential energy fluctuations can be described statistically by a Gaussian distribution $P(V)$[44–46,48] as $P(V) = 1/\sqrt{2\pi s^2}\exp(-V^2/2s^2)$, where V is the deviation from the average potential energy and s is the standard deviation indicating the strength of the potential energy fluctuations. These potential energy fluctuations result in a modified DOS of graphene, $D^*_{gr}(E)$, which can be obtained by the convolution of the DOS of ideal graphene, $D_{gr}(E)$, and the Gaussian distribution of potential energy fluctuations, $P(V)$, as[46]

$$D^*_{gr}(E) = \int_{-\infty}^{\infty} D_{gr}(E-V)P(V)dV = \frac{2}{\pi\hbar^2\upsilon_F^2}\left[E\,\mathrm{erf}\left(\frac{E}{\sqrt{2}s}\right) + \sqrt{\frac{2}{\pi}}s\exp\left(-\frac{E^2}{2s^2}\right)\right], \quad (5)$$

where $\hbar$ is the reduced Planck constant, υ_F is the Fermi velocity in graphene, and $\mathrm{erf}(x)$ is the error function given by $\mathrm{erf}(x) = (2/\sqrt{\pi})\int_0^x \exp(-t^2)dt$. The quantum capacitance in the presence of charged impurities can be calculated by replacing $D_{gr}(E)$ with $D^*_{gr}(E)$ in Eq. (4).

In the experiments, the measured quantity is the total gate capacitance C_g as a function of gate voltage V_g. C_g is given by $C_g^{-1} = C_{ox}^{-1} + C_Q^{-1}$ and V_g is related to V_{ch} by

$$V_g - V_{Dirac} = \left[V_{ch} + (1/C_{ox})\int_0^{V_{ch}} C_Q(V'_{ch})dV'_{ch}\right] \times |1 + i\omega C_g R_s|, \quad (6)$$

where we have included a series resistance R_s, as shown in the circuit diagram of Fig. 4(b). In Eq. (6), V_{Dirac} is the gate voltage at the Dirac point (where by definition $V_{ch} = 0$), i is the imaginary unit, and ω is the angular frequency of the small-signal gate voltage. The physical meaning of the series resistance R_s is the sum of the contact resistances and the resistances of the metal ring, the graphene sheet, and the silicon bulk. The parasitic impedance, which could result from factors such as fringing capacitances and a parallel conductance due to gate leakage, could be ignored because of the large device area and the small leakage current at the gate voltages used in the *C-V* measurements.

We have performed numerical calculations using Eqs. (4)–(6) to fit our experimental data for the 5 nm oxide. In these calculations, s and R_s were used as fitting parameters. The inset of Fig. 4(a) shows the zoom-in of the experimental capacitance dip observed under accumulation for the 5 nm oxide device, as well as the theoretical best-fit obtained with $s = 38$ meV and $R_s = 10.5$ kΩ. This value of s is in agreement with the values extracted from other experiments.[43,46,48] The good agreement between the experimental data and numerical calculations shows that the origin of the capacitance dip under accumulation observed for thin oxides is the quantum capacitance of graphene, taking into account the electrostatic potential fluctuations.

In addition to studying the effect of quantum capacitance, the *C-V* data at various oxide thicknesses can also be used to extract the workfunction of graphene,[13,20,23,25,26] which is another important parameter in the MOS device applications. Figure 4(c) shows the flat-band voltage (V_{FB}) of the MOS devices as a function of oxide thickness (t_{ox}). V_{FB} values were obtained by first calculating the flat-band capacitance (C_{FB}) of the MOS devices using $1/C_{FB} = (L_D/\varepsilon_{Si}) + (1/C_{ox})$,[25,26] where L_D is the extrinsic Debye length and ε_{Si} is the silicon permittivity. After calculating C_{FB}, the corresponding V_{FB} value can be obtained from the *C-V* data. The graphene workfunction can be extracted by[13,20,23,25,26]

$$V_{FB} = \Phi_{MS} - Q_f/C_{ox} = \Phi_{MS} - Q_f t_{ox}/\varepsilon_{ox}, \tag{7}$$

where Φ_{MS} is the graphene-Si workfunction difference and Q_f is the effective fixed oxide charge. As a result, from the *y*-intercept of the linear fit to the V_{FB} vs. t_{ox} data, as shown in Fig. 4(c), the graphene workfunction can be extracted as ~5.08 eV. The extracted graphene workfunction is at the high end of the range of values reported previously in the literature.[12,13,16,20,23,24] This could be due to *p*-type doping of the graphene layer[10,16] or interfacial charge traps at the graphene/oxide interface.[10,25,26]

In conclusion, we fabricated and characterized the MOS devices with graphene as the metal electrode. We demonstrated that Fowler-Nordheim tunneling dominates the gate current for SiO_2 thicknesses of 10 nm and above and extracted the F-N coefficients and the effective barrier height as a function of temperature. Furthermore, by performing *C-V* characterization, we observed a local minimum under accumulation for devices with thin oxides, which is due to the contribution of the quantum capacitance of graphene. Finally, we extracted the workfunction of graphene from the flat-band voltage at different oxide thicknesses. Our results provide important insights into the potential of graphene as a gate electrode in future MOS technology.

See supplementary material for the details of device fabrication, characterization, the energy band diagram, and additional *I-V* data.

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