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Ambipolar Thickness-Dependent Thermoelectric Measurements of WSe_2

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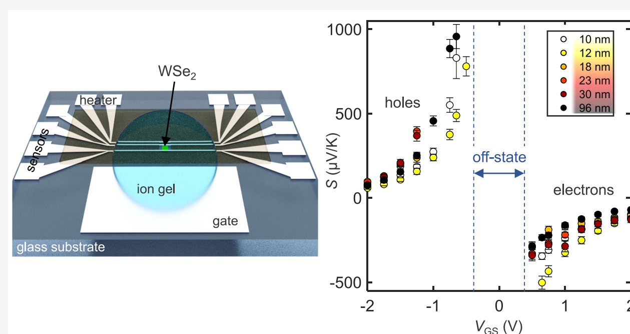
ABSTRACT: Thermoelectric materials can harvest electrical energy from temperature gradients, and could play a role as power supplies for sensors and other devices. Here, we characterize fundamental in-plane electrical and thermoelectric properties of layered WSe_2 over a range of thicknesses, from 10 to 96 nm, between 300 and 400 K. The devices are electrostatically gated with an ion gel, enabling us to probe both electron and hole regimes over a large range of carrier densities. We extract the highest *n*- and *p*-type Seebeck coefficients for thin-film WSe_2, −500 and 950 μV/K respectively, reported to date at room temperature. We also emphasize the importance of low substrate thermal conductivity on such lateral thermoelectric measurements, improving this platform for future studies on other nanomaterials.



KEYWORDS: *Seebeck coefficient, power factor, thin-film semiconductors, 2D materials*

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Over half of the energy generated by humanity is ultimately dissipated without being utilized, and the majority of that rejected energy is lost in the form of waste heat.[1] In this context, thermoelectric energy harvesting could play an important role, by converting spatial temperature gradients into an electrical voltage.[2] Most existing commercial thermoelectric devices are primarily based on Bi_2Te_3 and its related compounds; however, many of these materials are relatively inefficient and expensive.[3]

The efficiency of a thermoelectric material is quantified by its figure of merit, zT, which is defined as $zT = S^2\sigma T/\kappa$, where S is the Seebeck coefficient, σ is the electrical conductivity, T is the absolute temperature, and κ is the thermal conductivity. High zT can be achieved by maximizing the power factor PF = $S^2\sigma$ and minimizing κ. This can be accomplished by tuning the material's (electron or hole) carrier concentration, but because the constituent parameters of zT are interconnected, this can be a difficult process.[2] For example, S is often inversely proportional to the material's carrier density while σ is directly proportional. Therefore, increasing the carrier density can cause varying effects on zT, depending on the regime.

Another method to achieve more efficient thermoelectrics is to consider novel material systems. For example, low-dimensional materials with quantum confinement effects are uniquely suited to have efficient thermoelectric properties. Due to sharp features in their density of states, certain semiconducting two-dimensional (2D) materials could achieve large Seebeck coefficients,[4] boosting their PF. Furthermore, the dominant presence of interfaces and mass differences between constituent atoms in some 2D materials can lead to relatively low κ.[5,6] Although some theory and experiments have been done on 2D material thermoelectric properties, additional in-depth studies are required before these can be considered a viable commercial technology.[7−13]

In this work, we measure in-plane, thickness-dependent thermoelectric properties of WSe_2, probing both *n*- and *p*-type regimes. Among 2D materials, WSe_2 is relatively unique, as it is one of the few options that is readily ambipolar, either through gating or doping, which has also made it promising for nanoscale electronic applications.[14−16] Using ion gel gating, we can tune the Fermi level, evaluating S and σ over a range of carrier densities, mapping the PF through its peak value, which is difficult to accomplish with traditional back-gating through a thick oxide.[9,17] We extract peak room-temperature $S_p \approx 950 \pm 70$ μV/K for *p*-type and $S_n \approx -500 \pm 40$ μV/K for *n*-type, some of the highest reported values for WSe_2 to date at room temperature. This establishes WSe_2 as a promising candidate for applications such as temperature sensing, which benefit from higher induced voltages in a given temperature gradient.[18] Such large thermopower may also play a role in WSe_2 devices such as transistors or diodes, contributing to significant heating or cooling (and therefore a direct effect on

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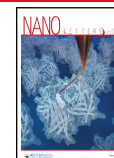

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their performance and reliability) depending on current flow direction.[19−21] For instance, due to the large Seebeck coefficient of WSe_2, one contact of a transistor may experience non-negligible thermoelectric heating while the other experiences cooling.[19]

In order to accurately measure the Seebeck coefficient of our WSe_2 films, it is important to sustain a constant, known temperature difference across the material. To accomplish this, we use a measurement structure whereby the WSe_2 samples are placed on a glass substrate, which has a low, uniform κ unlike the commonly used SiO_2/Si substrates.[22] The uniform κ of the substrate limits vertical heat flow, resulting in a longer and more gradual lateral temperature gradient, which enables a greater temperature difference to be sustained across the WSe_2 sample. This effect is quantified in Supporting Information section S1, with finite-element method simulations showing an ∼10× greater temperature difference (ΔT) across the sample when using a glass substrate. The larger ΔT, in turn, leads to a larger measurable Seebeck voltage, increasing the signal-to-noise ratio and reducing measurement error. In addition, the lower κ of the glass substrate reduces the lateral temperature drops within the thermometer lines, which, especially coupled with wide thermometer lines, can be a substantial source of error in the extracted Seebeck coefficient. Crucially, non-negligible thermometer line widths relative to the thermometer spacing, if not accounted for, can lead to a sizable underestimation of the true Seebeck coefficient, as we show in Supporting Information section S2. The Seebeck coefficients reported in this work have been corrected by the under-estimation factors listed in Table S1, which were computed using finite-element method simulations.

The WSe_2 samples are exfoliated from a bulk crystal using the "tape method" directly onto the glass substrates, and subsequently contacted with 40 nm of Pd deposited by electron-beam evaporation. An additional Pd line running parallel to WSe_2 contacts serves as the heater, as shown in Figure 1. While not in direct contact with the WSe_2 channel, this heater line is closely positioned and Joule-heated to create the lateral temperature gradient. All metal lines are ∼400 μm long, significantly longer than the width of the WSe_2 sample, to ensure a one-dimensional temperature gradient along its length rather than any temperature gradients along the width, which would confound the measurement.[23] The Pd lines in contact with the WSe_2 serve as the source and drain for electrical transport measurements, as well as the resistive thermometers. These metal lines (except for the channel area) are then capped with 100 nm evaporated SiO_2 for electrical insulation from the ion gel. Finally, a large Pd gate pad (with area on the order of ∼mm^2) is deposited on the same platform, such that the ion gel can simultaneously bridge the gate pad and the WSe_2 sample. A schematic of this device is pictured in Figure 1a, with a zoomed-in optical image in Figure 1b. The WSe_2 sample thicknesses are determined by atomic force microscopy (AFM) measurements.

To obtain the temperature difference across the WSe_2 sample, we calibrate our Pd lines by measuring their temperature coefficient of resistance (TCR). The four-point resistances of the Pd lines are measured as the sample temperature is increased above ambient, both along an increasing and decreasing temperature sweep to confirm the lack of hysteresis. The TCR is then extracted from a linear fit, as shown in Supporting Information section S3. Pd is chosen due to its chemical stability, linear TCR in the working temperature range, and good contact to WSe_2.[24−26]

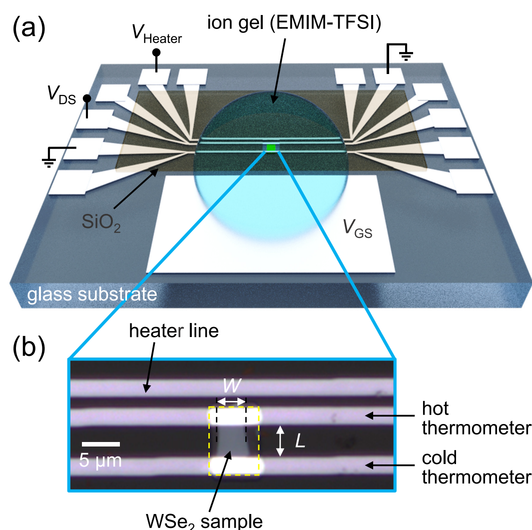

Figure 1. (a) Schematic of the electro-thermal measurement platform, on a glass substrate (not to scale). (b) Zoomed-in optical image of a WSe_2 sample with Pd contacts and heater line capped with 100 nm SiO_2 for electrical isolation. The dashed yellow line marks the window opened into the SiO_2, exposing the WSe_2 sample to the ion gel for electrostatic gating. The two thermometer lines in contact with the WSe_2 sample also serve as the source and drain for further electrical characterization. L is the sample length between thermometers, and W is the average WSe_2 sample width.

To modulate the carrier density and Fermi level, we use ion gel gating. This enables us to reach higher electron and hole densities on a glass substrate, which preserves a larger temperature difference between the thermometers than with commonly used SiO_2/Si substrates. The ionic liquid EMIM-TFSI (1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide), is mixed with PS−PEO−PS triblock copolymer and dissolved in acetonitrile before being deposited on the WSe_2 channel to form an ion gel for more structural stability. The sample is then cured in air at 80 °C for 10 min. The ion gel contacts the WSe_2 channel as well as the gate pad, such that an applied voltage on the gate pad leads to an electric field over the channel.

We first characterize the electrical properties of the WSe_2 devices. Representative transfer (I_D vs V_{GS}) and output (I_D vs V_{DS}) characteristics are shown for a 96 nm thick sample in Figure 2a and 2b, respectively. By using an ion gel for gating, we are able to sweep over a large range of carrier densities with a relatively small gate voltage range. This device shows nearly "perfect" ambipolar behavior [i.e., it conducts both with electrons (for positive V_{GS}) and holes (for negative V_{GS})] and does so with nearly the same maximum current for both electron and hole branches in Figure 2a. The maximum-to-minimum current ratio is $I_{max}/I_{min} \approx 10^8$, where I_{min} is limited by gate leakage and I_{max} reaches ∼3 μA/μm at V_{DS} = 100 mV.

Using these test structures and measurements, we investigate six different WSe_2 sample thicknesses, between 10 and 96 nm. Figure 3a displays the sheet conductance at each gate bias, $G_{sh} = (I_D/V_{DS}')(L/W)$, where W and L are the width and length of the sample, respectively, for the range of WSe_2 sample thicknesses investigated. The intrinsic voltage $V_{DS}' = V_{DS} - I_D R_{ser}$ subtracts out the series resistance R_{ser} caused by the long and thin Pd lines, which becomes a significant component

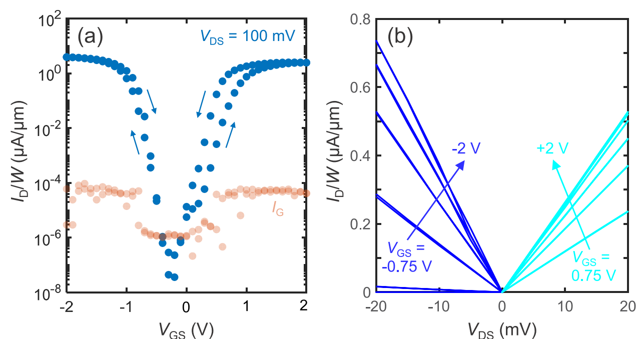

Figure 2. (a) Width-normalized measured transfer characteristics (I_D/W vs V_{GS}) of a WSe_2 sample that is 96 nm thick and 5 μm long, at room temperature. The gate leakage (light orange points) is minimized due to the SiO_2 layer insulating the metal lines from the ion gel. Small arrows mark voltage sweep directions. Hysteresis caused by the ion gel is minimized with a slow voltage sweep, 10 s at each data point. (b) Measured output characteristics (I_D/W vs V_{DS}) of the same sample, taken in V_{GS} increments of 0.25 V. Negative and positive V_{GS} are for hole and electron conduction, respectively.

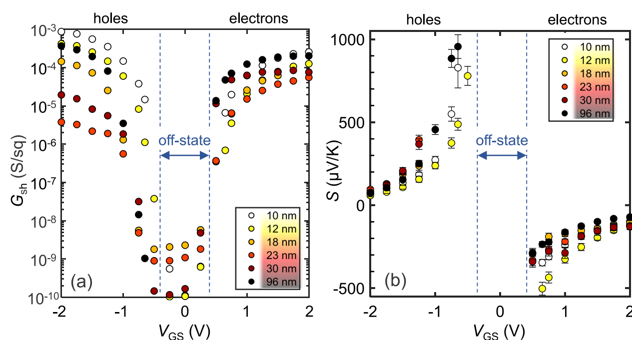

Figure 3. (a) Sheet conductance (G_{sh}) and (b) Seebeck coefficient (S) measured as a function of applied gate voltage (V_{GS}) for our WSe_2 samples of varying thicknesses, at room temperature. The S values are then adjusted based on finite-element method simulations, with error bars from both the simulations as well as the uncertainty in the thermovoltage measurements. Negative and positive V_{GS} voltage ranges are for hole and electron conduction, respectively. For low $|V_{GS}|$, when the Fermi level is in the band gap, the devices are in the off-state and no values for S are measured as the channel resistance begins to exceed the input impedance of the measurement tool.

when the channel is in the low-resistance on-state. These line resistances are measured in a 4-point configuration; their values are included in Supporting Information Table S3, and additional details are provided in Supporting Information section S4. As shown in Figure 3a, G_{sh} sharply drops for all devices in the off-state, at small $|V_{GS}|$ when the Fermi level is in the band gap. The WSe_2 channels are ambipolar and all show p- and n-type conduction, although any trend with thickness is not immediately apparent from these data.

During the Seebeck measurements, we apply a bias voltage across the heater line using a Keithley 2612 source-meter to Joule-heat it and create a lateral temperature gradient along the channel. We then measure the open circuit voltage induced across the WSe_2 with a Keithley 4200 while simultaneously varying the applied gate voltage. The measured Seebeck voltage is normalized over the temperature difference (calculated using the calibrated TCR values mentioned previously) to calculate the Seebeck coefficients. All reported Seebeck values are relative to the contact metal, Pd. To verify that the measured Seebeck voltage is not due to inadvertent electrical coupling effects, we confirm that it varies quadratically with the applied heater current, as expected for a temperature gradient induced by Joule heating.[9] Additionally, reversing the polarity of the applied heater current does not affect the measured Seebeck voltage. These verifications are discussed in Supporting Information section S5.

In Figure 3b, we plot the Seebeck coefficients for both electrons ($S_n < 0$) and holes ($S_p > 0$) over the range of our gate bias voltages. These values are measured with our electrothermal platform, and subsequently adjusted based on finite-element method simulations to account for the nonzero heater widths in the experiment design. As expected for a semiconductor, the absolute value of the Seebeck coefficient increases with decreasing carrier density,[27] reaching peak values of 950 μV/K for p-type (in the 96 nm thick sample) and -500 μV/K for n-type (in the 12 nm thick sample), at room temperature. These are the highest experimentally reported Seebeck coefficient values for thin-film WSe_2, exceeding those of bulk Bi_2Te_3, a commonly used commercial thermoelectric material.[3,28] Care must be taken in the Seebeck voltage measurement, as the input impedance of the measurement tool must be much greater than the device resistance for an accurate reading.[9] Therefore, no points are measured for the Seebeck coefficient when the devices are in their off-states, as indicated on Figure 3b.

While the electrical conductivity of the WSe_2 channel increases with increasing carrier density, the magnitude of the Seebeck coefficient follows the opposite trend. Thus, in order to gain a deeper understanding of the material's overall thermoelectric performance, we consider the PF, defined as $S^2\sigma$. As the electrical conductivity increases and there are additional charge carriers in the channel (either n- or p-type), the PF will first increase to a maximum point, and then subsequently decrease as the Seebeck coefficient drops when the Fermi level is pushed deeper into the conduction or valence band.[27]

The PF is plotted vs electrical conductivity in Figure 4 for each sample thickness. We find a maximum PF of 1200

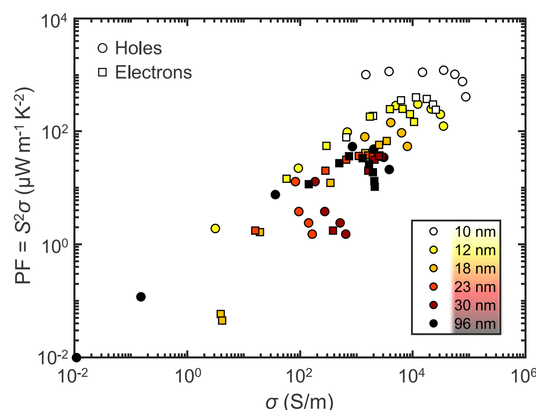

Figure 4. Plot of our calculated power factor (PF) vs electrical conductivity (σ) for WSe_2 samples of varying thicknesses. σ is normalized over each sample thickness. Circles represent holes and squares are for electrons. The PF (= $S^2\sigma$) for most data sets displays a clear maximum, which occurs because σ increases while S decreases at higher gate voltages and carrier densities. The high capacitance of our ion gel gating enables the sample conductivity and carrier density to be swept through this maximum point.

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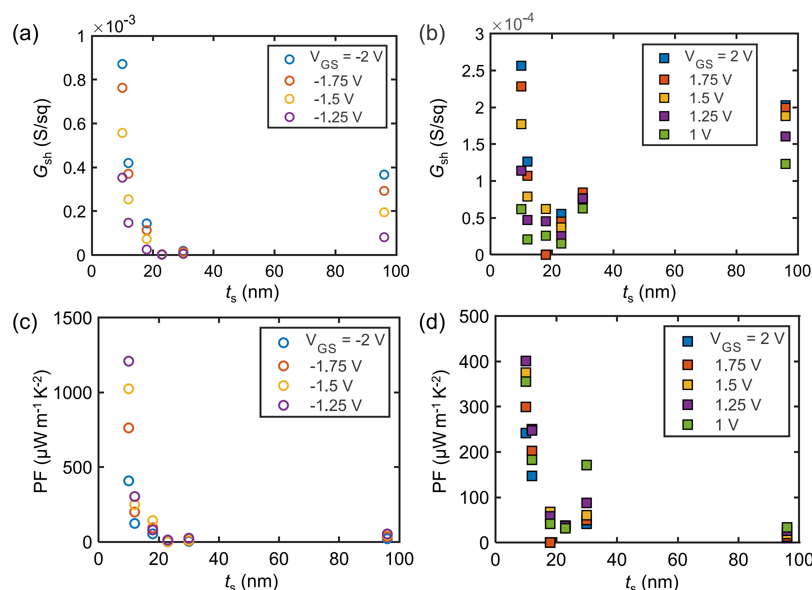

Figure 5. Sheet conductance (G_{sh}) vs sample thickness (t_s) for (a) holes and (b) electrons at several V_{GS} values. Power factor (PF) vs t_s for (c) holes and (d) electrons at several V_{GS} values, showing a general decrease of PF for increasing sample thicknesses.

μW m^{-1} K^{-2} for p-type conduction and 400 μWm^{-1}K^{-2} for n-type, both in the 10 nm thick WSe_2 sample. These PF estimates use the entire WSe_2 sample thickness (t_s) to calculate the electrical conductivity, $\sigma = G_{sh}/t_s$; however, the entirety of the sample is not conducting charge equally—rather, current flow is confined to a channel within the top few layers gated under the ion gel.[29,30] Therefore, if we considered only the thickness of the conducting channel in these calculations, the PF values would be substantially higher, comparable to the highest WSe_2 PFs reported to date. Supporting Information section S6 includes a PF analysis with an estimated conducting channel thickness, and Supporting Information section S8 presents a survey of WSe_2 Seebeck coefficients and PFs reported in existing literature.

Additionally, we consider the effect of the WSe_2 sample thickness on the measured electrical and Seebeck data. While the variation in G_{sh} may be in part due to device-to-device variation, there is a general trend of decreasing PF with increasing thickness for a given gate voltage. The maximum PF values we extract are for the 10 nm sample, and these roughly decrease for the thicker samples. Figure 5a and b plot G_{sh} vs sample thickness for holes and electrons, respectively. As expected, higher $|V_{GS}|$ leads to higher carrier densities and higher G_{sh}. Figure 5c and d display the PF vs sample thickness for electrons and holes, respectively, where we can see that the PF roughly decreases with increasing thickness. This can be partially explained by the electrical conductivity component of the PF—since σ is normalized by thickness, the thicker samples have lower average σ if the thickness of the conducting channel is limited to the surface layers of the sample. (Additional discussion of sample-to-sample variation is given in Supporting Information section S7.)

While quantum confinement in low-dimensional materials has long been recognized to boost the Seebeck coefficient and PF by introducing sharp features in the electronic density of states,[4,31−33] the WSe_2 samples used in this work ($\geq$10 nm thickness) are not thin enough to benefit from confinement along the cross-plane direction. However, we note that in the on-state, at the high electric fields enabled by the high-gate capacitance ion gel, the charge carriers that are responsible for conduction are in fact confined in a near-triangular field-induced potential well at the surface of WSe_2. The width of this potential well, and the thickness of the 2D electron gas formed therein, are on the order of nanometers.[13,30] It has been experimentally shown in other materials that this field effect-induced quantum confinement can lead to an enhancement in Seebeck coefficient.[34−36]

Therefore, thicker WSe_2 samples do not have inherently lower Seebeck coefficients than thinner samples in the thickness regime probed here, if they are electrostatically surface-gated to tune the carrier density. We expect that this, coupled with good material quality, is the reason that values of S we extract here are higher than those reported for monolayer or few-layer WSe_2,[8,13] and that the PFs we calculate are likewise competitive (see Supporting Information Table S5). Like these previous studies,[8,13] we are also unable to determine the κ of our substrate-supported devices, which are ill-suited for such a measurement. However, the in-plane κ of WSe_2 in our thickness range is expected to be between 2 and 40 Wm^{-1}K^{-1} near room temperature,[6,37] with the larger values corresponding to thicker samples with fewer defects. More accurate κ investigations for samples in the thickness range considered here (~10 to 96 nm) are possible on larger suspended samples and should be the focus of future work.

In conclusion, we investigated fundamental thermoelectric properties for layered WSe_2, sweeping through a range of carrier densities for both electrons and holes and measuring the highest reported Seebeck coefficients for this material. Our on-chip measurement platform demonstrates the advantages of utilizing a low thermal conductivity substrate to preserve a greater temperature difference along the WSe_2 channel, and the use of an ion gel for electrostatic gating allowed for a high degree of control over Fermi level tuning. These results, as well as the ability of WSe_2 to support both n- and p-type conduction, make it a promising candidate for thermoelectric applications such as temperature sensing. In addition, the large Seebeck coefficients uncovered here also mean that significant

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heating or cooling may occur at WSe_2 device (e.g., transistor) contacts, depending on current flow direction.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.2c03468.

Finite-element method simulations quantifying the substrate thermal conductivity impact on the resultant temperature gradient; finite-element method simulations to correct for Seebeck coefficient underestimation due to non-negligible thermometer widths; temperature coefficient of resistance (TCR) calibrations; discussion of additional measured data; band gap (E_G) analysis; comparison of data with literature; temperature-dependent measurements. (PDF)

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Author Contributions

V.C. and E.P. conceived the idea and wrote the manuscript with inputs from all authors. V.C. and H.R.L. designed the experiments, and fabricated and measured the samples. C.K. performed the finite-element method modeling. C.J.M. and A.D. provided insights on the measurement setup and data analysis.

Notes

The authors declare no competing financial interest.

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Supporting Information

Ambipolar Thickness-Dependent Thermoelectric Measurements of WSe_2

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Section S1. Substrate Impact on the Temperature Difference across a Flake

To highlight the importance of the choice of substrate in the thermal design of the test structure, we have performed thermal finite-element method simulations for a cross-section of the test structure (Figure S1). For the same heater temperature, we compare the temperature differences, ΔT, between the two thermometer lines for the glass substrate used in this work [Figure S1(a)] and a substrate with 300 nm-thick SiO_2 on Si [Figure S1(b)] similar to those used in other studies.[1,2] The high thermal conductivity Si substrate ($\kappa_{Si} \approx 140$ W/m/K for undoped Si near room temperature) acts like a thermal ground, causing the temperature at the top of the sample to drop close to ambient temperature (T_0) within a short distance (comparable to the SiO_2 thickness) from the heater line. This causes the temperatures on both thermometer lines, as well as their difference, to be much less than the heater temperature.

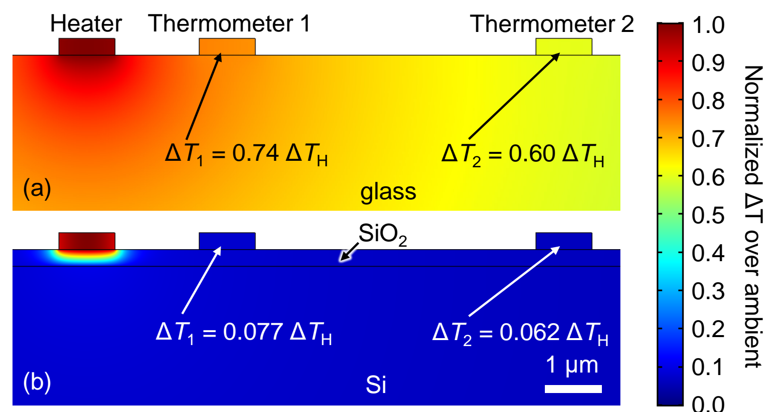

Figure S1. Temperature rise (ΔT) normalized by the peak heater temperature rise (ΔT_H) in the vicinity of the heater and thermometer lines for typical heater-thermometer line spacings, with (a) the glass substrate used in this work, and (b) a typical substrate with 300 nm-thick SiO_2 ($\kappa_{SiO2} = 1.4$ W/m/K) on Si. The temperature rise is normalized to the peak temperature rise in the heater line. The bottom of the substrate is assumed to be at ambient temperature, T_0. The thermometer temperature differences ($\Delta T_1 - \Delta T_2$) in (a) and (b) are 14% and 1.5% of ΔT_H, respectively. The thicknesses of the metal lines have been exaggerated for this visualization (300 nm instead of the 40 nm thickness used in the experiments and simulation).

This problem can be largely avoided by using a uniform substrate such as glass, for which ΔT between the thermometer lines is close to 10× that with the SiO_2/Si substrate. The low thermal conductivity of glass ($\kappa_{glass} \approx 0.8$ W/m/K) is also beneficial for preventing a large temperature drop within thermometer lines, as they are much higher in thermal conductivity than the substrate. This is important for an accurate measurement of the Seebeck coefficient: see section S2 on measurement error these temperature drops contribute.

Section S2. Effect of Thermometer Widths on Seebeck Coefficient Measurements

Extracting the Seebeck coefficient as the ratio of the measured thermometer potential difference to the measured temperature difference implicitly assumes that the separation of the thermometer lines is much greater than the thermometer widths (2.4 μm). However, due to the limited sizes of our exfoliated WSe_2 samples, the distances between the closest edges of the thermometer lines are 2.5 to 5.9 μm (see Table S3), short enough that the thermometer widths are not negligible. In this section, we quantify this error and explain how to properly estimate the Seebeck coefficients based on our measurements.

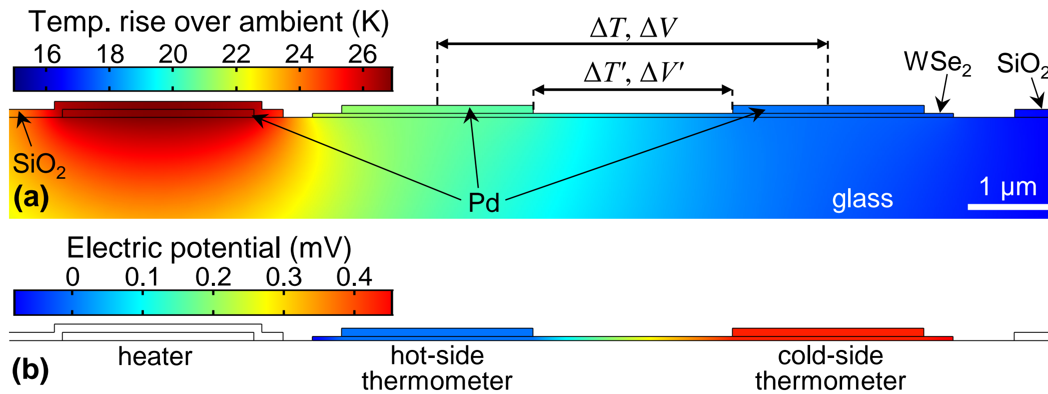

Figure S2. Electrothermal simulation results for the sample with 2.5 μm channel and 18 nm thick WSe_2 film, showing (a) the temperature rise over ambient, and (b) the electric potential along the device cross section. The Pd line on the left is the heater and the two Pd lines on the right are the thermometers. The thicknesses of the Pd lines and WSe_2 are exaggerated for better visualization. A Seebeck coefficient of 200 μV/K was assumed. The thermal properties assumed are the nominal values listed in Table S2.

Figure S2 shows electrothermal simulation results for the device with the shortest channel (2.5 μm, on the 18 nm thick WSe_2 film), for which the measurement error is consequently highest. ΔT and ΔV refer to the temperature and potential differences between the centers of the thermometer lines, respectively, while $\Delta T'$ and $\Delta V'$ are the temperature and potential differences between the inner edges of the thermometers (2.5 μm apart for this particular device), as defined in Figure S2. The thermometer temperatures are measured via the electrical resistance, which is inversely proportional to the metal conductivity averaged within the thermometer cross section, and thus approximately proportional to the average metal resistivity. Since the resistivity changes approximately linearly with temperature rise, the electrically measured temperature corresponds to the average temperature within the thermometer. Assuming the temperature gradient within each thermometer is roughly uniform, this average is close to the temperature at the center of the thermometer. Consequently, ΔT is approximately equal to the experimentally measured temperature difference ΔT_{avg} between the thermometers, and S $\Delta V/\Delta T_{avg} \cong \Delta V/\Delta T$ thus represents the measured Seebeck coefficient.

Under the thermometer lines, the effective Seebeck coefficient of the Pd/WSe_2 stack is

$$S' = \frac{G_{\mathrm{WSe2}} S + G_m S_m}{G_{\mathrm{WSe2}} + G_m} = \frac{G_{\mathrm{WSe2}}}{G_{\mathrm{WSe2}} + G_m} S \ll S,$$

where S and S_m are the WSe_2 and metal Seebeck coefficients, and G_{WSe2} and G_m are the WSe_2 and metal sheet conductances, respectively. Here, we have taken $S_m = 0$ since we measure the Seebeck coefficient S relative to that of the Pd thermometers, and also used the fact that $G_m \gg G_{WSe2}$.

The measured Seebeck voltage is

$$\begin{aligned} \Delta V &= \Delta V' + S'(\Delta T - \Delta T') \\ &= S\Delta T' + S'(\Delta T - \Delta T') \\ S &= \frac{\Delta V - S'(\Delta T - \Delta T')}{\Delta T'} \cong \frac{\Delta V}{\Delta T'} \end{aligned}$$

where we have used $S' \ll S$. Letting $\delta T = \Delta T - \Delta T'$, which is the sum of the temperature drops from the center of each thermometer to its inner edge,

$$S \cong \frac{\Delta V}{\Delta T - \delta T} = \frac{\Delta V}{\Delta T} \frac{1}{1 - \frac{\delta T}{\Delta T}} \cong \frac{S_{meas}}{1 - \frac{\delta T}{\Delta T}} \tag{S1}$$

Equation S1 shows that the true Seebeck coefficient is greater than the measured Seebeck coefficient ($S_{meas} = \Delta V/\Delta T_{avg}$) by a factor of $1/(1 - \delta T/\Delta T)$, which depends on the temperature drops across the thermometer lines. To calculate these corrections, we have performed electrothermal finite-element method simulations for all six devices, and the results are listed in Table S1, where the uncertainties in the factor $\delta T/\Delta T$ are due the to the uncertainties in various thermal properties, the ranges of which are included in Table S2. The Seebeck coefficients we report in the manuscript are the values corrected by the factors and uncertainties listed in Table S1, after the raw Seebeck coefficients are measured as $\Delta V/\Delta T_{avg}$. Device 3 with the shortest channel (2.5 μm) requires the largest correction, as expected. Thermometer line widths must be taken into account when designing such experiments and extracting results, and for our set of thermometer widths and separations, these errors range from 17 to 30%.

Table S1. Factors by which raw Seebeck coefficients extracted as $\Delta V/\Delta T_{avg}$ underestimate the true Seebeck coefficient. The details of the device geometries, such as the flake thicknesses, are listed in Table S3.

Device number	1	2	3	4	5	6
***δT*/Δ*T* (%)**	17 ± 4	21 ± 5	30 ± 7	20 ± 5	26 ± 6	22 ± 4

Table S2. Material and interface thermal properties used in simulations. Ranges of parameters considered for uncertainty estimation are indicated in parentheses. Due to lack of data the thermal boundary resistance ranges for WSe_2 were chosen to include those measured for other interfaces of WSe_2, as well as interfaces of other transition metal dichalcogenides such as MoS_2. The thermal conductivity range considered for Pd is lower than bulk values to account for the reduced thermal conductivities of thin metal films.

Material	**Thermal conductivity ($Wm^{-1}K^{-1}$)**
WSe_2[3, 4]	25 (15 – 40)
Pd	50 (30 – 70)
glass[9]	0.8
SiO_2[10]	1.4

Material interface	**Thermal boundary resistance (Km^2/GW)**
WSe_2 – Pd[5-8]	62.5 (31 – 125)
WSe_2 – glass[5-8]	62.5 (31 – 125)

Finally, rather than calculating $\Delta V/\Delta T_{avg}$ directly in simulations, we may instead calculate $\delta T/\Delta T$ from simulated temperatures only (i.e. with no regard to simulated potential differences, without having to model the thermoelectric effects) to approximate the Seebeck coefficient underestimation factor, in accordance with Eq. S1. We find that doing so yields estimates that are within 1.5% of the underestimation factors given in Table S3, which confirms the validity of Eq. S1 and the approximations that lead to it. This also confirms that Seebeck coefficient underestimation arises from the non-negligible temperature drops along the widths of the thermometer lines, which in turn are caused by the fact that these widths are not negligible compared to the channel length.

Section S3. Temperature Coefficient of Resistance (TCR) Calibration

To quantify the temperature gradient induced by the metal heater line along the sample, we measure the four-point resistance of each Pd thermometer line at elevated temperatures by uniformly heating the substrate on a heated stage. The TCR is calculated as:

$$\alpha = \frac{R - R_0}{R_0(T - T_0)}$$

where α is the TCR, R is the measured resistance, R_0 is the resistance of the line at ambient temperature, T is the temperature, and T_0 is the ambient temperature.

Figure S3 shows plots of R/R_0 vs. $\Delta T = T - T_0$ for the two metal thermometer lines on each device, with dashed lines representing the linear fit from which the TCR is extracted. Although the TCR for thin Pd is well characterized in the literature, small nonidealities in the deposition and fabrication processes may cause the value to deviate slightly, and so it is still important to calibrate each line individually. The values are compiled in Table S3, and all fall within the expected range.[11]

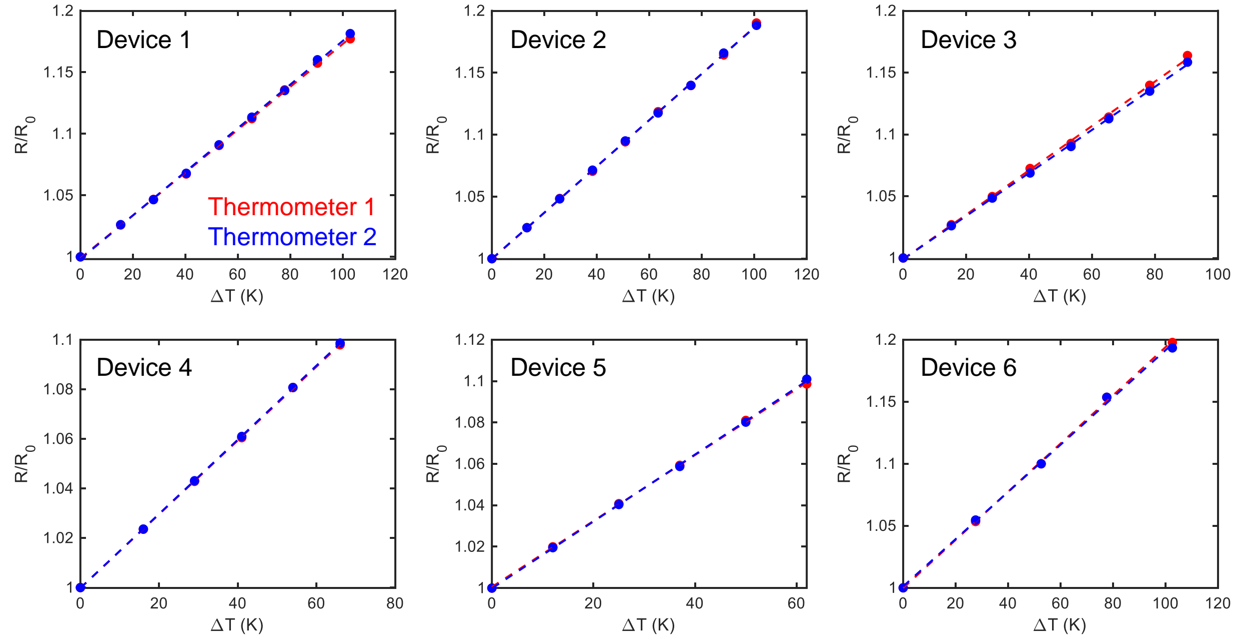

Figure S3. TCR calibrations for each of the two Pd thermometer lines on six devices. The four-point resistance is measured for each line at room temperature and elevated temperatures, and the ratio of the measured resistance (R) to the room temperature resistance (R_0) is plotted against the temperature increase. The dashed lines represent linear fits of the data, and the slopes of these lines are the TCRs. The TCRs are listed in Table S3 below.

Table S3. Compiled device information

WSe$_2$ Device Parameters				Pd Line Parameters			
Device	**Thickness (nm)**	**Width (μm)**	**Length (μm)**	**TCR$_{line1}$ (K^{-1})**	**TCR$_{line2}$ (K^{-1})**	**R$_{line1}$ (Ω)**	**R$_{line2}$ (Ω)**
1	10	3.7	5.9	1.74×10^{-3}	1.77×10^{-3}	1104	1157
2	12	5.6	4.2	1.87×10^{-3}	1.86×10^{-3}	961	997
3	18	3.8	2.5	1.80×10^{-3}	1.74×10^{-3}	1202	1389
4	23	5.6	5.4	1.49×10^{-3}	1.50×10^{-3}	1440	1622
5	30	3.9	3.5	1.59×10^{-3}	1.62×10^{-3}	1420	1593
6	96	13.6	5	1.94×10^{-3}	1.90×10^{-3}	938	1030

In Table S3, we tabulate the physical dimensions of each exfoliated WSe_2 sample, measured using atomic force microscopy (AFM). Although all Pd lines are nominally the same thickness of evaporated material, small differences in the processing conditions or imperfections in patterning may lead to differences in their TCR values and resistances. Therefore, we individually calibrate TCR values for each line separately and compile them in Table S3. There is some variation, however the measured TCR values are within a reasonable range for thin, evaporated Pd.[11]

Table S4. Absolute temperature rises over WSe_2 samples

Device	ΔT_{line1} (K)	ΔT_{line2} (K)	ΔT_{across} (K)
1	14.7	10.6	4.1
2	12.9	10.1	2.8
3	19.9	14.8	5.1
4	22.7	16.6	6.1
5	21.0	16.8	4.2
6	13.1	9.9	3.2

In Table S4, we list the absolute temperature increases measured at the two Pd thermometer lines (ΔT_{line1} and ΔT_{line1}) when the heater current is applied, as well as the temperature difference between them (ΔT_{across}). We note that the total temperature differences across the WSe_2 samples (ΔT_{across}) are large enough to measure an appreciable induced thermovoltage, yet small enough such that we are able to neglect the Thomson effect from our analysis.

Section S4. Sheet Conductance Calculation Details

Due to the relatively long and thin Pd lines used as the source and drain contacts to the WSe_2 samples, there is a series resistance added to the WSe_2 channel resistance that becomes especially significant when the channel is in the on-state. Therefore, to more accurately estimate the sheet conductance (G_{sh}) of the samples, we subtract the Pd line resistances as shown in the diagram of Figure S4 below. We apply a drain-to-source voltage (V_{DS}), calculate the actual voltage drop across the WSe_2 (V_{DS}'), then use this V_{DS}' value to calculate G_{sh}. Here,

$$V_{DS}' = V_{DS} - I_D \frac{R_{line\,1}+R_{line\,2}}{2}, \text{ and therefore } G_{sh} = \frac{I_D}{V_{DS}'}\frac{L}{W}.$$

The four-point resistance values for each Pd line at room temperature are included in Table S1.

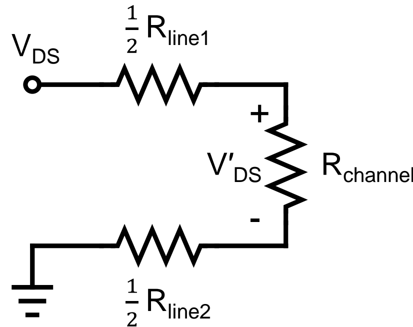

Figure S4. A simplified circuit diagram showing the current path through half of one Pd line, through the WSe_2 channel, and out through the other half Pd line.

Section S5. Measured Thermovoltage vs. Heater Current

When measuring low voltage values, we validate that these are from the thermovoltage, and not from spurious signals. In Figure S5, we plot the measured voltage between the source and drain contacts (i.e. the two parallel thermometer lines) against the heater current. Because Joule heating is directly proportional to I^2R and the Seebeck voltage is directly proportional to the temperature gradient, the measured voltage should be approximately quadratic with respect to the heater current. This relationship is confirmed in Figure S5.

Additionally, we further verify that the measured voltage is not due to leakage from the heater line by reversing the direction of the heater current and noting that the measured thermovoltage value does not change, in magnitude or sign.

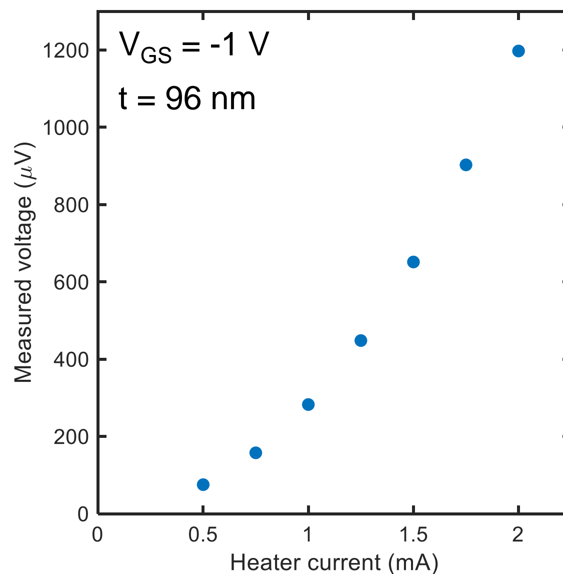

Figure S5. The voltage measured between the source and drain contacts of a 96 nm thick WSe_2 sample biased at a gate-source voltage $V_{GS} = -1$ V, plotted as a function of the applied heater current.

Section S6. Power Factor (PF) Calculation Considering Conducting Channel Thickness

In a 2D, multilayered transistor, the layers contributing to conduction are a subset of the total number of layers, and the specifics depend on the channel thickness as well as the applied gate-source voltage.[12] In this analysis, we make a rough estimate that the majority of the current flows through the top two layers of the samples, and thus, we recalculate the PFs using this "effective" channel thickness (t_{eff}), where t_{eff} = 1.3 nm.[13,14] As shown in Figure S6, the adjusted PF values for each device follow the same trend, increasing with electrical conductivity to a maximum and turning over as the Seebeck coefficient decreases. However, the PFs are higher when only t_{eff} is considered, peaking at ~9300 µW/m/K^2 for holes and ~3100 µW/m/K^2 for electrons in the 10 nm sample. Compared to the values in Table S5 (further below), this represents one of the highest PF values for a *p*-type layered 2D material.

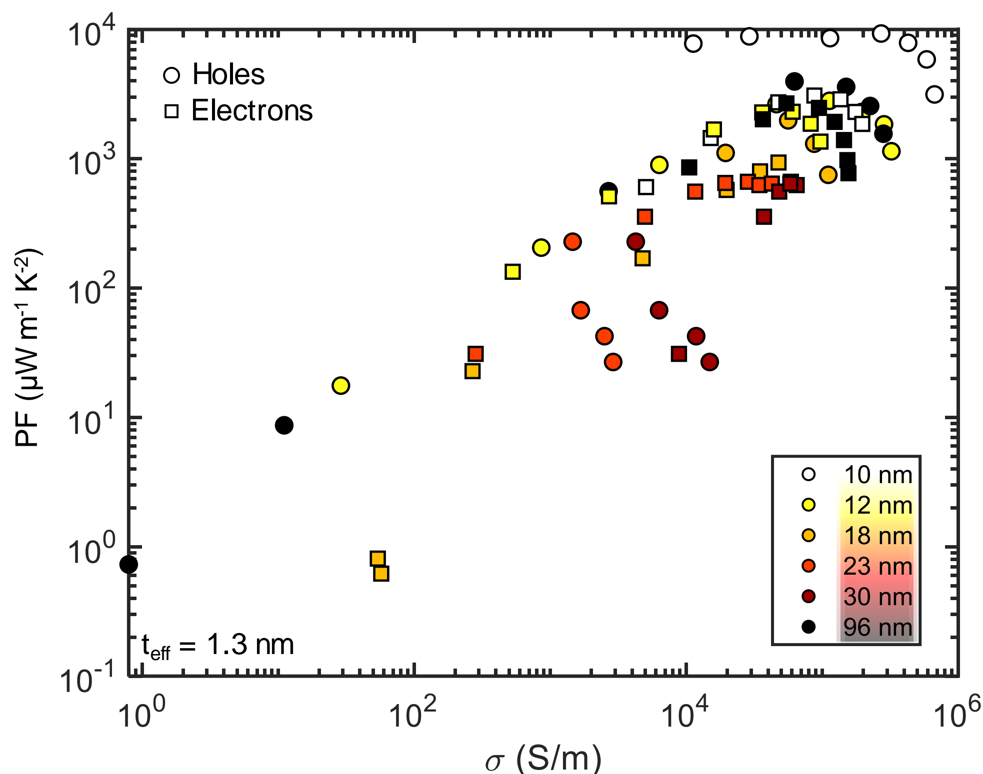

Figure S6. Power factor (PF) plotted against electrical conductivity (σ), where σ is calculated using an "effective" channel thickness, t_{eff} = 1.3 nm.

Section S7. Estimating Electrical Band Gap Variations Between Devices

For a high enough gate capacitance, the difference between the *n*- and *p*-branch threshold voltages at low V_{DS} in our ambipolar WSe_2 can be used to roughly approximate the material band gap.[15] We perform this extraction from the transfer characteristics of our devices and plot the sheet conductances (G_{sh}) against E_G in Figure S7(a) and (b) for holes and electrons, respectively. Devices with higher extracted E_G values tend to have lower G_{sh} for a given V_{GS}, and consequently, the PF values are also lower, as shown in Figure S7(c) and (d). While the Seebeck coefficient depends on the shape of the band structure, which contributes to the effective mass of the carriers, it is not directly dependent on E_G itself. Although the range of extracted E_G values is larger than expected for the sample thicknesses here (due to device-to-device variation), the overall trend is consistent with wider band gap samples having a lower PF.

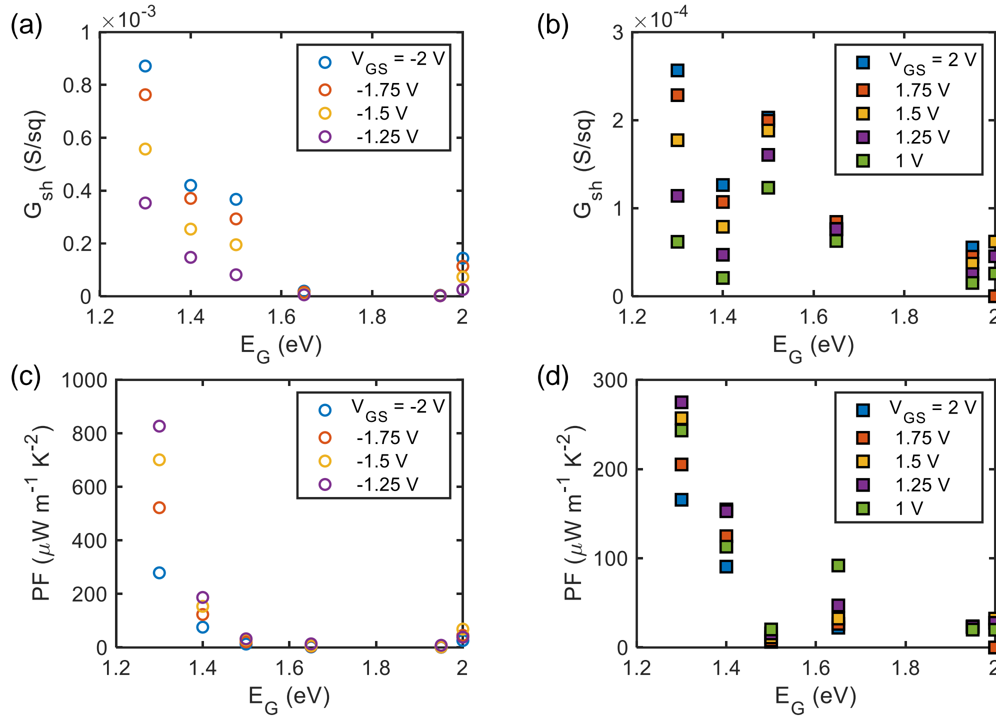

Figure S7. Plots of G_{sh} for (a) holes and (b) electrons as well as PF for (c) holes and (d) electrons against the estimated E_G, extracted from the transfer characteristics of the flakes. There is a general trend of G_{sh} decreasing with increasing extracted E_G, and therefore a corresponding decrease in PF.

Section S8. Comparison of Our Results with Existing Literature

The second row of Table S5 below contains values from our work, and subsequent rows contain a compilation of other thermoelectric studies of semiconducting 2D materials. The maximum Seebeck coefficient and power factor (PF) values reported in these works are listed, along with the material type, thicknesses measured, and further pertinent details. In the last column, we list the method used to gate the material and modulate its carrier density.

From this table, we note that Seebeck coefficients that are orders of magnitude higher than the median reported value are at very low carrier densities, such that the power factor would likely be too low for use in efficient thermoelectric energy harvesting. Additionally, for 2D materials specifically, it is important to distinguish between the total material thickness vs. the thickness that is conducting charge—these values will differ for multilayer systems and affect the estimation of electrical conductivity. Our reported Seebeck coefficient is one of the highest obtained for a *p*-type 2D material, and our PF values are competitive with other works when only the thickness of the conducting channel (t_{eff}) is considered.

Table S5. Comparing these results to literature values

Ref.	Material	Thicknesses Studied	$\|S\|$ (µV/K)	PF (µW/m/K^2)	Gating
This work	WSe_2	10-96 nm	950 (p-type, 96 nm) 500 (n-type, 12 nm)	1200 (p-type, 10 nm) 400 (n-type, 10 nm)	EMIM-TFSI
M. Kayyalha et al.[1]	MoS_2	1-23 layers	500 (n-type, 4 layers)	5000 (n-type, 2 layers)	300 nm SiO_2/Si
M. Yoshida et al.[13]	WSe_2	3 layers*	~300 (p-type, 3 layers) ~280 (n-type, 3 layers)	3200 (n-type) 3700 (p-type)	DEME-TFSI
Hippalgaonkar et al.[2]	MoS_2	1, 2, 3 layers	~520 (n-type, 2 layers)	8500 (n-type, 2 layers)	275 nm SiO_2/Si
S. Timpa et al.[16]	WSe_2	~3-4 nm (4-6 layers)	180 (n-type, 6 layers) 160 (p-type, 4 layers)	2400 (p-type, 4 layers)	40-60 nm hBN/Au/280 nm SiO_2/Si
J. Pu et al.[17]	MoS_2, WSe_2	monolayer	380 (p-WSe_2) 250 (n-WSe_2) 160 (n-MoS_2)	300 (p- WSe_2) 100 (n- WSe_2) 200 (n- MoS_2)	EMIM-TFSI
M. Buscema et al.[18]	MoS_2	monolayer	1×10^5 (n-type**)	Not reported	285 nm SiO_2/Si, laser heating
J. Wu et al.[19]	MoS_2	monolayer	3×10^4 (n-type***)	Not reported	285 nm SiO_2/Si
Y. Saito et al.[20]	BP	40 nm	510 (p-type****)	460 (p-type)	DEME-TFSI
S. Choi et al.[21]	BP	10 and 30 nm	400 (p-type)	Report “sheet” PF	300 nm SiO_2/Si
J. Fleurial et al.[22]	Bi_2Te_3	Bulk (3 mm)	250 (n-type) 230 (p-type)	Not reported	Annealed to vary carrier concentrations
M. Saleemi et al.[23]	Bi_2Te_3	Bulk, nanostructured	120 (n-type)	2800 (n-type)	None

*to calculate σ, only the thickness of the conducting channel, 1.3 nm, is considered
**Seebeck value is measured for a very low carrier density
***at 280 K and at very low carrier density
****at 210 K

Section S9. Temperature-Dependent Electrical and Seebeck Measurements

For the thinnest two WSe_2 samples in this work, we carry out temperature-dependent electrical and Seebeck coefficient measurements, which are summarized in Figure S8 below. Transfer characteristics as well as Seebeck coefficients are plotted for 296 K (both in the beginning and again after cooling back down), 350 K, and 400 K. The temperature range we measure over is restricted due to limitations of the ion gel used. At higher temperatures, the ion gel becomes more conductive and leakage currents increase[24]; in turn, any current through the ion gel causes measurements to become unreliable. These measurements confirm that the WSe_2 sample characteristics are consistent and stable between room temperature and 400 K. Additionally, these values do not include the corrections from the finite-element method simulations, which were not performed for higher temperatures.

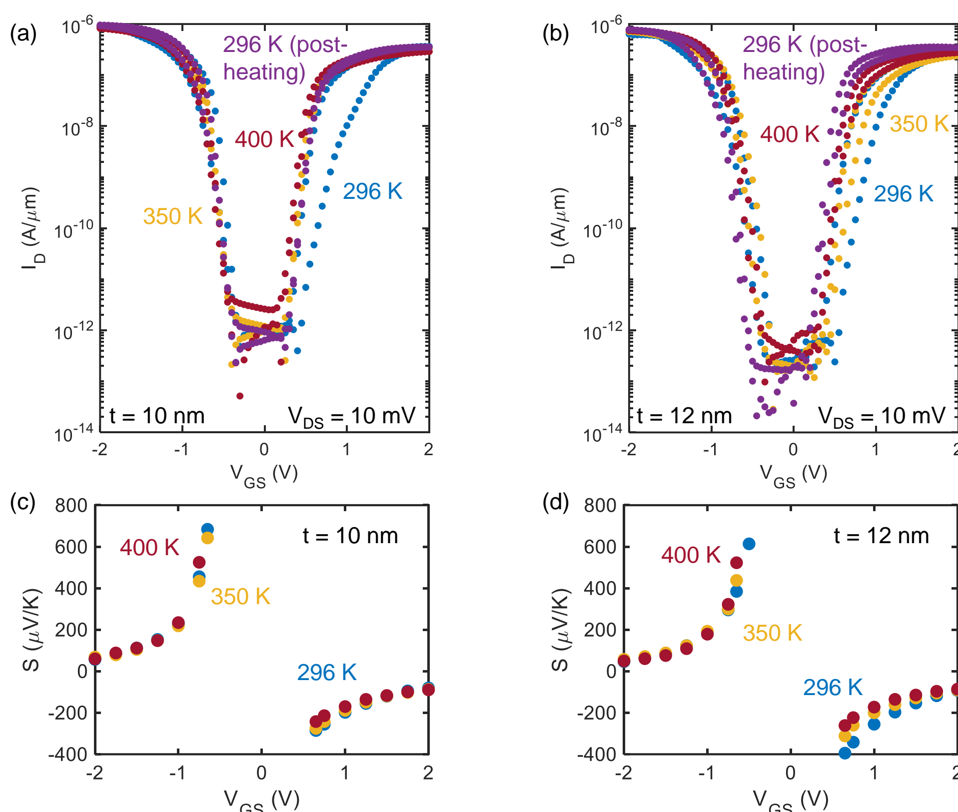

Figure S8. Temperature-dependent transfer characteristics for (a) 10 nm and (b) 12 nm thick WSe_2 samples, and Seebeck coefficients for the same (c) 10 nm and (d) 12 nm thick samples. Use of the ionic liquid limits our temperature range between approximately room temperature and 400 K to ensure stable measurements.

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