Effect of Back-Gate Dielectric on Indium Tin Oxide (ITO) Transistor Performance and Stability

Alwin Daus, *Member, IEEE*, Lauren Hoang, *Graduate Student Member, IEEE*, Carlo Gilardi, *Member, IEEE*, Sumaiya Wahid, *Graduate Student Member, IEEE*, Jimin Kwon, *Member, IEEE*, Shengjun Qin, Jung-Soo Ko, Mahnaz Islam, *Graduate Student Member, IEEE*, Aravindh Kumar, Kathryn M. Neilson, *Graduate Student Member, IEEE*, Krishna C. Saraswat, *Life Fellow, IEEE*, Subhasish Mitra, *Fellow, IEEE*, H.-S. Philip Wong, *Fellow, IEEE*, and Eric Pop, *Fellow, IEEE*

***Abstract*— Amorphous oxide semiconductors (AOSs) are receiving increased attention for electronics requiring low fabrication temperatures, but concerns remain about their stability. Here, we fabricate thin (∼4 nm) indium tin oxide (ITO) field-effect transistors (FETs) with three back-gate dielectrics (HfO_2, Al_2O_3, SiO_2) deposited under various conditions. We find that low dielectric surface roughness <1 nm ensures good ITO channel mobility, high dielectric breakdown field, and reduced trap states as confirmed by our simulations. The FET subthreshold drain current is accurately described by incorporating both interface and ITO bulk donor traps into the simulations. We also study the ITO devices under positive bias stress (PBS), finding the highest stability with HfO_2 dielectrics, which contrasts reports on other AOS transistors. Through benchmarking, we identify lowering the equivalent oxide thickness (EOT) as one of the major contributors for improved PBS stability. These findings elucidate several key parameters for the improvement of AOS FET performance and stability.**

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Alwin Daus is with the Department of Electrical Engineering, Stanford University, Stanford, CA 94305 USA. He is now with the Department of Microsystems Engineering (IMTEK), University of Freiburg, 79110 Freiburg, Germany.

Lauren Hoang, Carlo Gilardi, Sumaiya Wahid, Jimin Kwon, Shengjun Qin, Jung-Soo Ko, Mahnaz Islam, Aravindh Kumar, Kathryn M. Neilson, Krishna C. Saraswat, H.-S. Philip Wong, and Eric Pop are with the Department of Electrical Engineering, Stanford University, Stanford, CA 94305 USA (e-mail: epop@stanford.edu).

Subhasish Mitra is with the Department of Electrical Engineering and the Department of Computer Science, Stanford University, Stanford, CA 94305 USA.

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***Index Terms*— Amorphous oxide semiconductor (AOS), bias stress stability, field-effect transistor (FET), gate dielectric, indium tin oxide (ITO), interfaces, mobility, traps.**

I. Introduction

AMORPHOUS oxide semiconductors (AOS) are widely used for field-effect transistors (FETs) in displays and are candidates for electronics on various substrates enabled by low-temperature processing (<400 °C) [1]. Thus, they have attracted increased attention for monolithic 3-D integration [2], especially because high ON/OFF current ratio (>10^9) and high drive currents (>1 mA/μm) have been shown in thin, short-channel AOS FETs [3], [4], [5]. Thin indium-tin-oxide (ITO) is one AOS candidate with good mobility ∼50 $cm^2\,V^{-1}\,s^{-1}$ and low contact resistance ∼160 $\Omega{\cdot}\mu$m having been reported [4], [5]. However, the impact of the gate dielectric material on ITO FET performance and bias stress stability remains unknown. Here, we investigate the properties of ITO FETs with several ∼10 nm thick back-gate dielectrics grown by various atomic layer deposition (ALD) conditions. We find that low root-mean-square (RMS) roughness (Δ_{rms} < 1 nm) and low equivalent oxide thickness (EOT) of the dielectric are both important to obtain high effective mobility (μ_{eff}), low subthreshold swing (SS) including steep near-threshold turn-on, and improved bias stress stability. Based on our results, we conclude that HfO_2 dielectrics and interfaces are preferable over Al_2O_3 for ITO FETs, which contrasts recent findings on FETs with other AOS [6], [7].

II. Device Fabrication and Characterization

Fig. 1(a) displays a schematic and an optical image of the fabricated transistors. First, local Ti/Pd (5/35 nm) back-gates were deposited by electron-beam evaporation onto thermally oxidized silicon (∼300 nm SiO_2 on Si) and patterned by lift-off. Then, ∼10 nm HfO_2 (thermal or plasma), Al_2O_3 (ozone), or SiO_2 (plasma) were grown on the back-gates by

TABLE I

COMPARISON OF DIFFERENT HIGH-κ DIELECTRICS ALL DEPOSITED BY ALD AT 200 °C FOR BACK-GATED ITO FETS: t_{de} DIELECTRIC THICKNESS; κ RELATIVE DIELECTRIC PERMITTIVITY; μ_{eff} EFFECTIVE MOBILITY; V_T THRESHOLD VOLTAGE; SUBTHRESHOLD SWING; D_{it} INTERFACE TRAP DENSITY. THE INITIAL ROUGHNESS (Δ_{rms}) OF THE BARE SiO_2/Si SUBSTRATE AND Ti/Pd BACK-GATE METAL WERE <0.2 AND ~0.3 nm, RESPECTIVELY. THE ITO DEPOSITION DOES NOT FURTHER INCREASE THE ROUGHNESS OF THE RESPECTIVE ALD-COVERED ELECTRODES

Dielectric	t_{de} (nm)	Δ_{rms} (nm)	κ	Break-down field (V/nm)	μ_{eff} ($cm^2/V/s$) at ~$8x10^{12}$ cm^{-2}	V_T (V)	Min. SS (mV/decade)	D_{it} (cm^{-2}/eV)
HfO_2 (therm-1)	11	1.7	16.6	0.52	21	1	83	$4.0x10^{12}$
HfO_2 (therm-2)	10.5	0.7	16.2	0.65	45	-0.6	79	$2.4x10^{12}$
HfO_2 (plasma)	9.5	0.5	15	0.72	43	0.2	78	$2.1x10^{12}$
Al_2O_3 (ozone)	11	0.4	7.6	0.85	44	0.2	97	$2.4x10^{12}$

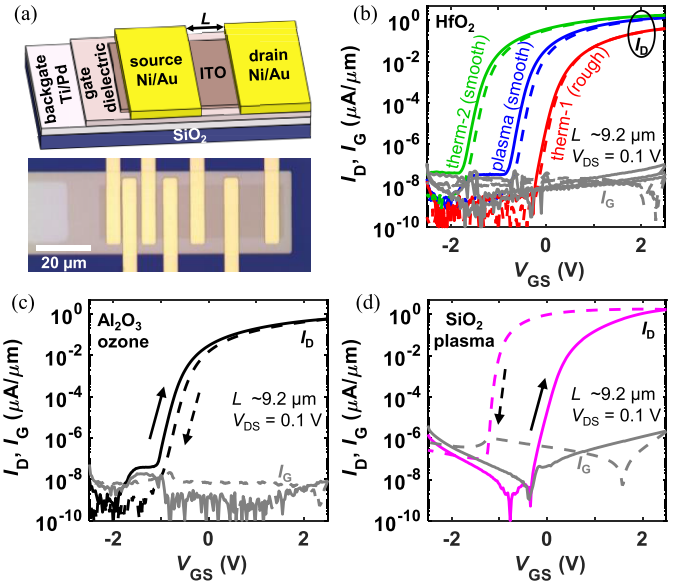

Fig. 1. Back-gated ITO FETs. (a) Device schematic and optical image of TLM structure with channel lengths L from ~0.2 to 9.2 μm. Measured transfer characteristics (I_D–V_{GS}) with (b) HfO_2 (several types), (c) Al_2O_3, and (d) SiO_2 gate dielectrics all grown by ALD, with physical thicknesses from 9.5–11 nm. I_G is the gate leakage and small arrows mark the forward and backward voltage sweep directions, indicating greater hysteresis for devices with SiO_2 dielectric.

ALD at 200 °C. We note two thermal-ALD HfO_2 films were tested with different tools, one with higher (therm-1) and the other with lower surface roughness (therm-2, see Table I). Subsequently, ~4 nm ITO was deposited by radio frequency magnetron sputtering at room temperature (100 W, 5 mTorr, 9:1 Ar/O_2 ratio) and channels were defined by wet etching in aqueous (1.7%) HCl solution. The ITO films are amorphous (as confirmed by X-ray diffraction) and are not expected to become crystalline when annealed up to 350 °C [5]. Finally, Ni/Au (40/20 nm) source/drain contacts were electron-beam evaporated and patterned by lift-off.

Devices with varying source-drain separation (i.e., channel lengths, L) were characterized on a probe station in the dark, in ambient air. Metal-oxide-semiconductor capacitors were used to measure the dielectric capacitance in accumulation, extract the relative dielectric constant (κ), and determine the breakdown field. Positive bias stress (PBS) was investigated on FETs keeping the source/drain grounded while applying the stress voltage to the gate. The dielectric and ITO thickness and roughness were verified by atomic force microscopy. The threshold voltage (V_T) and μ_{eff} were extracted by linear extrapolation at peak transconductance and from transfer length method (TLM) structures [Fig. 1(a)], respectively. Within the channel lengths considered here (0.2–9.2 μm) we do not see a difference in PBS, D_{it}, and minimum SS. Thus, we focus the bulk of our analysis on the longest channels to mainly probe the semiconductor/dielectric interface and minimize any contact effects.

III. RESULTS AND DISCUSSION

Fig. 1(b)–(d) display drain current I_D versus gate–source voltage V_{GS} characteristics of our ITO FETs with different gate dielectrics. The devices with HfO_2 and Al_2O_3 have reasonably low hysteresis (<0.2 V). In contrast, devices with SiO_2 show pronounced counterclockwise hysteresis with increased gate current I_G and a peak in I_G that coincides with a sub-60 mV/decade SS in the reverse sweep direction attributed to charge de-trapping in the imperfect insulator [8], [9]. Thus, we deduce that the quality of our ALD SiO_2 process is insufficient, and we focus our attention instead on the high-κ dielectrics. Comparing the devices with HfO_2 dielectrics from various processes [Fig. 1(b)], we find significant V_T variation, which indicates differences in fixed dielectric charges.

Furthermore, the RMS roughness is notably higher for the film "therm-1" leading to half the μ_{eff} of other films, which all have similar $\mu_{eff} > 40$ $cm^2\,V^{-1}\,s^{-1}$ (Table I, with values averaged from each two TLMs). This illustrates the importance of smooth surfaces for few-nm thick AOS to exhibit good mobility, similar as reported for back-gated organic transistors [10]. Moreover, the lower dielectric roughness can also be correlated with higher breakdown fields observed (see Table I). The dielectric permittivities of all high-κ dielectrics are within typical ranges (Table I), with that of Al_2O_3 being about half of HfO_2, which also leads to a higher minimum SS and lower drive current (compared to the "smooth" HfO_2).

We now turn our attention to the SS and D_{it} for the dielectrics with smooth surfaces, which lead to FETs with good $\mu_{eff} \geq 40$ $cm^2\,V^{-1}\,s^{-1}$. We fit the experimental transfer

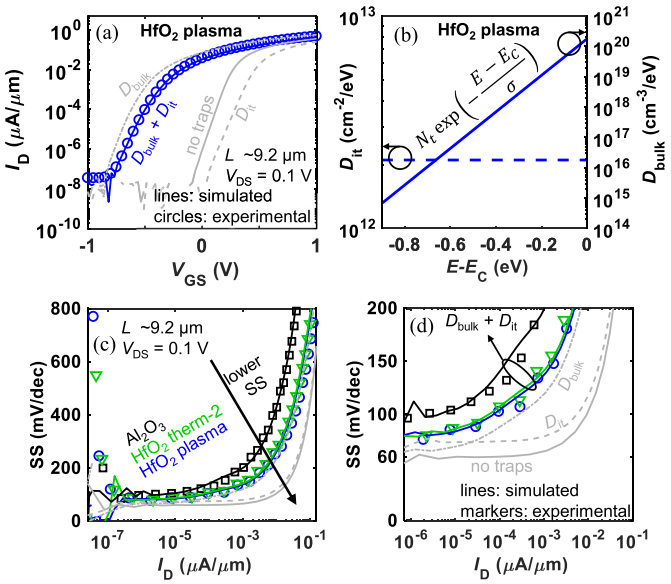

Fig. 2. TCAD simulation and SS. (a) Transfer characteristic of an ITO FET with plasma-HfO_2 dielectric. The subthreshold region is accurately fit by introducing an interface trap density D_{it} and an ITO bulk donor trap density D_{bulk}. (b) Trap densities corresponding to (a), showing an exponential decay of D_{bulk} from the conduction band edge and a constant D_{it}. The subthreshold region of the FETs is fit with the parameters for density (N_t) and slope (σ) of bulk traps and D_{it}. (c) SS versus I_D for FETs with different dielectrics and the TCAD fitting. (d) Zoomed-in low SS region of (c) showing that D_{it} dominates the deep SS region and D_{bulk} limits the near-threshold region. Simulation parameters [5], [12], [13], [14], [15]: κ (ITO) = 9, electron effective mass (ITO) = 0.3, valley degeneracy = 2, band gap = 3.7 eV, and electron affinity = 4.3 eV. We use the same D_{bulk} for all three fits shown in (c) and (d). Other parameters are noted in Table I.

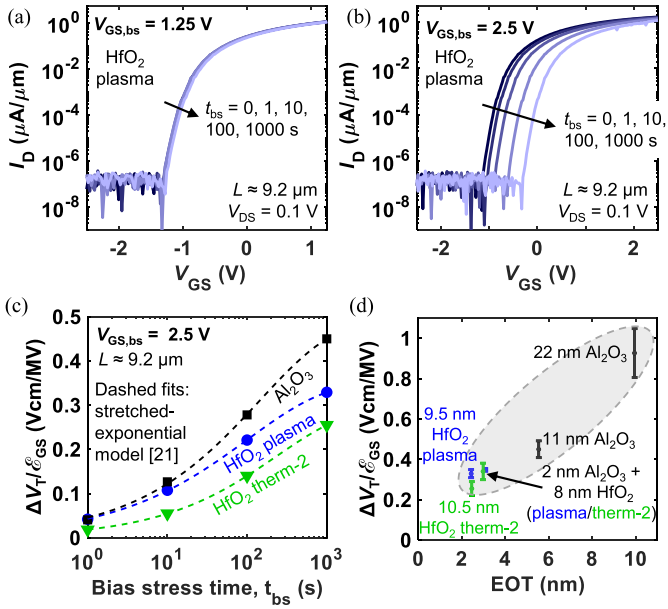

Fig. 3. Transfer characteristics of two FETs with plasma-HfO_2 dielectric after bias stress $V_{GS,bs}$ of (a) 1.25 V and (b) 2.5 V, for increasing bias stress times t_{bs}. (c) ΔV_T normalized by vertical field $\mathcal{E}_{GS}$ versus t_{bs}. (d) $\Delta V_T/\mathcal{E}_{GS}$ versus EOT for our AOS FETs stressed for 1000 s including data from [22]. The devices were stressed at similar $\mathcal{E}_{GS}$ ~2.5 MV/cm, but ΔV_T is normalized because of variations in physical thicknesses.

characteristics with Sentaurus TCAD [11] [Fig. 2(a)]. A reasonable representation of the subthreshold region is achieved by incorporating a constant, effective interface trap density D_{it}, and an ITO bulk donor trap density D_{bulk} as fitting parameters [Fig. 2(b)], along with material parameters from the literature [5], [12], [13], [14], [15]. There are several types of sub-gap states possible in AOS and they depend on process conditions like annealing and AOS deposition method [16], [17], [18]. However, for our purpose, we simplify our modeling assumptions and only use donor-type bulk traps, known to be caused by oxygen deficiencies, also a source of n-type doping in AOS [16]. We believe this is reasonable because such defects are well-established for AOS, and we also note that the nature of sub-gap states has only minor effects on our D_{it} extraction, such that our conclusions about the dielectrics are not affected. Moreover, the constant D_{it} [Fig. 2(b)] is a simplified effective representation to compare our different devices sufficient for the scope of this study.

For simplicity, because we focus on the SS and the near-threshold region, we neglect the effect of deep traps on V_T. Therefore, we shifted the simulated transfer characteristics in Fig. 2(a) by a fixed voltage to align to experimental data. Nevertheless, we note that the introduction of donor states negatively shifts V_T because the (ionized) states act as dopants and increase carrier density. In contrast, a small positive V_T shift is observed when adding interface states where electron trapping occurs, electrostatically delaying device turn-on.

We extract similar D_{it} values for the different dielectrics, with plasma-HfO_2 being slightly lower than others (Table I). Overall, the SS with HfO_2 dielectrics is lower than with Al_2O_3 because of the higher κ, which is evident especially at higher I_D [Fig. 2(c)] but also noticeable for the minimum SS (Table I). It is interesting to note that D_{it} mostly influences SS in the deep subthreshold regime, while D_{bulk} dominates the near-threshold behavior [Fig. 2(d)]. We have assumed the same D_{bulk} ($N_t = 1.8 \times 10^{20}$ cm^{-3}, $\sigma = 72$ meV) when fitting devices with "smooth" dielectrics, but devices with "rough" HfO_2 were fit with larger D_{bulk} ($N_t = 2.6 \times 10^{20}$ cm^{-3}, $\sigma = 72$ meV) and D_{it} (Table I) indicating more defects both in ITO and at the ITO/HfO_2 interface. This highlights that the AOS quality also impacts the subthreshold characteristics. The shallow donor-like tail states can be linked to undercoordinated metal atoms (or oxygen vacancies), which are influenced by AOS stoichiometry as well as process conditions such as annealing [16], [19].

Last, we perform PBS measurements. We find that V_T shifts positively due to the trapping of electrons near the dielectric/semiconductor interface (e.g., within dielectric defect states) [8], [20], where higher stress voltage causes larger shifts [Fig. 3(a) and (b)]. The dependence of ΔV_T on bias stress time follows a stretched-exponential form [Fig. 3(c)] [21], with fit maximum $\Delta V_T/\mathcal{E}_{GS}$ of ~0.7, ~0.9, and ~1.1 V·cm/MV for "therm-2" HfO_2, plasma HfO_2, and Al_2O_3, respectively.

Our ITO FETs with HfO_2 dielectric are more stable than those with Al_2O_3 dielectric, in contrast to a previous study of IGZO [7] which used Al_2O_3 dielectrics for improved stability. This could be due to variations in electron affinity dependent on AOS type and thickness, causing different energy separations between conduction bands and defect bands in Al_2O_3 and HfO_2 [20]. We note that PBS is more affected by

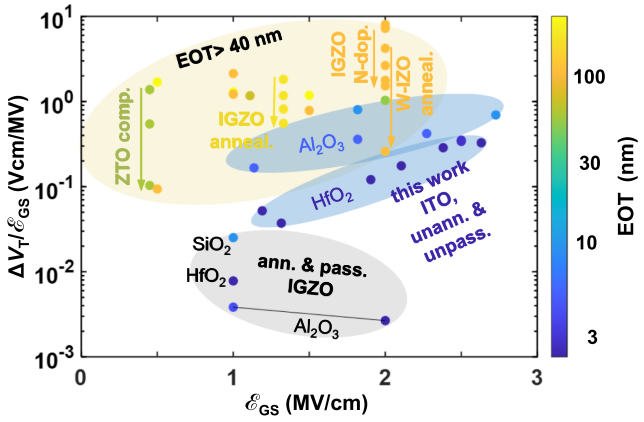

Fig. 4. Benchmarking of $\Delta V_T/\mathcal{E}_{GS}$ for AOS FETs stressed for 1000 s. The orange-shaded area with EOT $>$ 40 nm contains several AOS including ZnSnO (ZTO), InGaZnO (IGZO), W-doped InZnO (W-IZO), InAlZnO, and In_2O_3. The arrows denote that annealing, N-doping, or composition can improve stability. Our work with ITO indicates higher stability with HfO_2 dielectrics (thermal and plasma), while a recent IGZO work shows higher stability with Al_2O_3. Literature data: [7], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32].

dielectric bulk traps than by interface traps (D_{it}) [20]. Thus, it is reasonable that devices with "therm-2" HfO_2 (Table I) have slightly higher D_{it} and lower $\Delta V_T/\mathcal{E}_{GS}$ than devices with plasma HfO_2.

Based on our data, we find that EOT strongly affects PBS [Fig. 3(d), with averages and standard deviations for each 2–3 devices] [22]. This is supported by our benchmarking plot where we compare $\Delta V_T/\mathcal{E}_{GS}$ and EOT from various works on AOS FETs [Fig. 4] [7], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32]. In fact, reducing dielectric thickness and/or increasing the dielectric permittivity suffices to lower ΔV_T. If the trapped charge is uniformly distributed in the dielectric, reducing the dielectric thickness (and EOT) naturally eliminates part of the trapped charges [33]. If the trapped charge is at a fixed distance from the channel interface (e.g., as a simplified scenario after bias stress), we can write [34]

$$\Delta V_T = -\frac{(t_{de} - d_{tr})Q_{tr}}{\kappa \varepsilon_0}$$

where t_{de} is the physical gate dielectric thickness, d_{tr} is the fixed distance between the traps and the channel interface, $Q_{tr} < 0$ is the trapped charge, κ is the relative dielectric constant, and ϵ_0 is the vacuum permittivity. Thus, when EOT is reduced (i.e., t_{de} is reduced or κ is increased), the gate electrode is more effective at screening the trapped charge [35]. The equation above also reveals that there can be some exceptions when combinations of t_{de} and κ lower EOT but not ΔV_T.

Nevertheless, we also note there are more effects influencing AOS stability under PBS: the AOS composition is believed to be a factor, where metal dopants with high bond-dissociation energy suppress the formation of excessive oxygen vacancies [36], which could also be the case for Sn in ITO [37]. The addition of dopants like W has shown to improve stability, but lower AOS mobility [36]. Other factors for stability are process parameters like annealing and passivation as indicated in Fig. 4. In addition, for some dielectrics, the release of residual hydrogen can lead to negative V_T shifts upon PBS due to n-doping of the channel [16], [28].

This indicates that AOS stability is a multidimensional problem, where the whole device stack and fabrication process need optimization. We believe that scaled EOT is one of the major factors, independent of AOS composition, and highly stable AOS FETs may be achievable without sacrificing mobility.

IV. Conclusion

We have studied ~4 nm thin, back-gated ITO transistors with different dielectrics and have found that low $\Delta_{rms} < 1$ nm is important to obtain good mobility and reduced bulk and interface trap densities. We highlight the correlation between surface roughness and bulk trap densities, which is important for optimizing ITO devices. We also identify EOT as an important parameter for improved PBS stability, both within our work and via benchmarking with the literature. Future studies on annealing and passivation could lead to further improvements in the electrical stability and performance of ITO transistors.

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