Temperature-Dependent Contact Resistance to Nonvolatile Memory Materials

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***Abstract*— Emerging nonvolatile memories store data by reversible resistive switching in phase-change materials or metal oxides. As memory cell dimensions are reduced to ~10-nm scale or below, electrical contacts can dominate the device behavior, yet are often poorly understood. Here, we study the contact resistance to memory materials $Ge_2Sb_2Te_5$ (GST), TiO_2, and HfO_2 with low-current and temperature-dependent measurements. We find that the contact resistivity varies over ten orders of magnitude depending on the material; contact resistivity to cubic GST is near $10^{-2}\Omega\cdot cm^2$ (~1000 times greater than the hexagonal GST) while that to HfO_2 is as high as $5 \times 10^5 \Omega\cdot cm^2$ at room temperature. Contact resistivity decreases with increasing temperature and with increasing current density, the latter due to the non-Ohmic nature of the contacts. These results are important to understand the design, scaling, and behavior of nanoscale data storage devices.**

***Index Terms*— Contact resistance, nonvolatile memory, phase-change memory (PCM), resistive random-access memory (RRAM).**

I. Introduction

NONVOLATILE memory technologies such as resistive random-access memory (RRAM) [1]–[3], phase-change memory (PCM) [4]–[6], and spin-transfer torque memory [7] are emerging candidates for data storage with their simple metal–insulator–metal (MIM) device structure. To increase storage capacity and to enable logic-memory integration, it is essential to scale individual memory cells below ~10 nm

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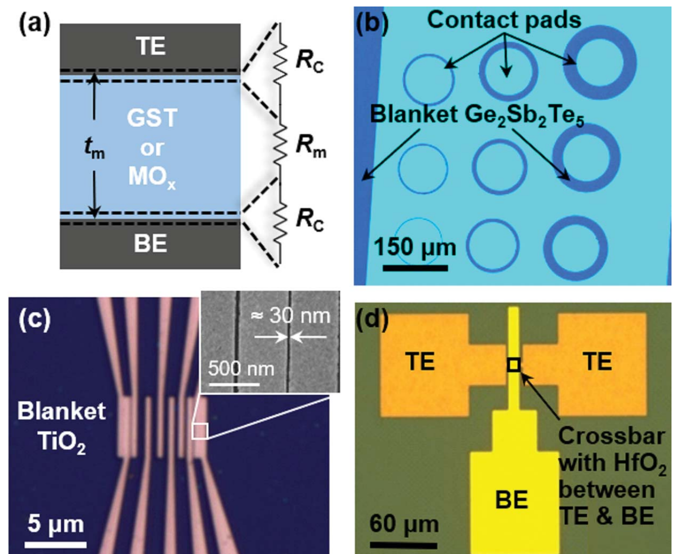

Fig. 1. (a) Schematic of the typical resistive memory cell, showing the TE, BE, and memory material thickness (t_m). Resistive contributions of the switching material (R_m) and contacts (R_C) are also displayed. Optical images of contact resistance test structures used in this work. (b) C-TLM. (c) L-TLM structure with minimum contact spacing down to ~30 nm (inset). (d) Multiple crossbars with varying material thicknesses (t_m) used for V-TLM test structures.

and to stack them in three-dimensional (3-D) arrays [8]. The energy efficiency of these arrays demands minimizing read–write energies at the cell level [6], [9]. For nanoscale RRAM and PCM, the contact resistance can become a significant component of overall cell resistance [6], [10]. Thus, within sub-10-nm 3-D stacked memory cells, both the switching material resistance (R_m) and the contact resistance (R_C) to the switching layer, as shown in Fig. 1(a), could determine the ultimate performance and energy efficiency limits of such data storage technologies.

These memory technologies rely on reversible (high versus low) resistance states of a material to store information. PCM typically uses $Ge_2Sb_2Te_5$ (GST), with electrically controllable transitions between different material phases. Metal oxides [MO_x in Fig. 1(a)] such as HfO_2 and TiO_2 are the materials of choice for switching in RRAM because of sub-10-nm filamentary conduction. The metal electrodes to PCM and RRAM materials perform an active role in the device switching behavior. For example, GST devices rely on heat confinement at the nanoscale metal contacts to improve energy efficiency [11],

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while ion migration toward contacts can lead to eventual PCM device failure [12]. Metal interfaces to the switching oxide in RRAM devices can determine whether device behavior is unipolar or bipolar [13] and volatile or nonvolatile [14]. These observations suggest a need to understand such memory contacts at a fundamental level.

Previous work has estimated the electrical contact resistance of GST with TiW [15], TiN [16], and other metal nitrides [17]. Contacts to TiO_2 [18] and HfO_2 [19] have not yet been measured, in part because conduction in these materials is a combination of thermionic emission, tunneling, and trap-assisted transport. Such non-Ohmic conduction makes separation of bulk and interface components difficult. Moreover, in all these memory materials, the extraction of electrical contact resistance is challenging because of its high values, often comparable with the instrumentation resistance.

In this study, we utilize circular [20], linear [21], and vertical transfer length measurement (V-TLM) [17] structures [Fig. 1(b)–(d)] to extract the bulk and contact resistance over the temperature range from 300 to 450 K, for the three memory materials considered. The different structures help us extract interface properties for materials with bulk resistivities varying over 14 orders of magnitude. For example, we show linear TLM (L-TLM) measurement down to ∼30-nm contact spacing for TiO_2 films; however, such lateral measurements are challenging for films with high resistivity ($>10^{10}\Omega\cdot$cm), for example as-deposited HfO_2 (before forming). We overcome this problem by measuring vertical devices with different HfO_2 thicknesses in an effective V-TLM [17]. Consequently, this study includes the first such extraction for average contact resistivity to as-deposited HfO_2 thin films. To contextualize our results, the contact resistivities for RRAM oxides are ≈10 orders of magnitude higher than for typical semiconductors like silicon.

II. Test Structure Fabrication

Thermal noise considerations at room temperature (RT ≈ 296 K) and measurement instrument limitations demand maximum resistance $R_{\max} \approx 100$ TΩ across all test structures. To keep measured resistances below this value, thin-film resistivity for GST ($\rho_m < 10^3\Omega\cdot$cm), TiO_2 ($<10^3\Omega\cdot$cm), and HfO_2 ($<10^{14}\Omega\cdot$cm) indicates different upper limits on test structure dimensions. To achieve material-specific dimensions, we fabricate circular TLM (C-TLM) for blanket 30-nm GST films, L-TLM for blanket 10-nm TiO_2 films, and V-TLM for 7.5 to 12.5-nm-thick HfO_2 films (see Fig. 1).

GST and TiO_2 films were deposited using a load-locked plasma sputter tool on 90-nm SiO_2 on Si substrates. GST deposition required a direct current (DC) plasma from a GST target at 25 W in a 3-mtorr Ar ambient for a deposition rate ∼5–6 nm/min. TiO_2 thin films were deposited with reactive sputtering from a Ti target in a 28:2 Ar:O_2 ambient in radio-frequency (RF) plasma at 150 W and 3 mtorr. Both films were deposited at RT, and thus, the initial films were amorphous. Patterning of C-TLM pads [Fig. 1(b)] on the 30-nm GST used optical lithography (with no liftoff layer to minimize residue, and no O_2 plasma descum to limit the oxidation of the GST), while L-TLM structures on the 10-nm thin TiO_2 films used electron beam (e-beam) lithography [Fig. 1(c)]. Poly(methyl methacrylate) used for e-beam patterning on TiO_2 leaves negligible residue, which is verified by e-beam imaging in the inset of Fig. 1(c). Then, 2-nm Ti and 50-nm Pt were e-beam-evaporated on both samples, followed by metal liftoff by successively dissolving resists in *N*-methyl pyrrolidone (NMP), acetone, and isopropanol (IPA). The same contact metal was used in both cases for the sake of consistency. An additional set of C-TLM test structures for GST with pure Pt contacts was fabricated in the same manner for comparison. The contacted GST and TiO_2 samples were annealed at 180 °C for 1 h in vacuum, which crystallizes the GST into the cubic (fcc) phase.

For the V-TLM structures [Fig. 1(d)], the bottom electrode (BE) was first patterned on 90-nm SiO_2 on Si substrates by optical lithography, then metallized with 2-nm Ti/50-nm Au, and lifted off in NMP, acetone, and IPA. On the top surface of the patterned Au for three different samples, blanket HfO_2 films of three thicknesses ($t_m = 7.5$, 10, and 12.5 nm) were deposited by atomic layer deposition (ALD) in a load-locked system at 200 °C. Then, a blanket 20-nm TiN film was deposited as the top electrode (TE) on all three samples at the same time, by reactive RF sputtering from a Ti target in Ar:N_2 ambient. This was followed by optical lithography to pattern the TE shape, contact pads, e-beam evaporation of 60-nm Au, and liftoff. The patterned Au was used as an etch mask for the blanket TiN under a Cl_2+ SF_6 plasma, forming the TE. Stoichiometries for all films were confirmed by X-ray photoemission spectroscopy (XPS). We note that C-TLM control structures were fabricated for TiO_2 and HfO_2 films as well. However, in order to achieve measurable current levels within lithography constraints (such as contact spacing versus line-edge roughness for large contact widths), we found L-TLM and V-TLM better suited for TiO_2 and HfO_2 measurements, respectively. We performed all electrical measurements less than one day after fabrication, in vacuum ($< 5 \times 10^{-5}$ torr) to minimize the effects of surface oxidation and moisture.

III. Measurements With Test Structures

A. C-TLM on GST Films

We extract the temperature-dependent contact resistance to our fcc-GST films using the C-TLM structures shown in Fig. 1(b). Extraction of contact resistivity using C-TLM requires taking into account the effect of the circular contact geometry. The resistance dependence on the contact spacing (d) follows the relation [20]:

$$\frac{R}{c} = \frac{\rho}{t_m}\frac{d}{\pi D} + 2R_C = \frac{\rho}{t_m}\frac{d}{\pi D} + \frac{2\rho_C}{A} \quad (1)$$

where R is the measured resistance, D (= 200 μm) is the diameter of the center contact, d ($\ll D$) is the spacing between the center and the outer contact, $c = D(2d)^{-1}\ \ln(1 + 2d/D)$ is the correction factor for the circular geometry, t_m is the thickness of the GST film, ρ is the thin film resistivity, ρ_C is the temperature- and current-dependent average contact resistivity, and A is the effective contact area. Assuming the current transfer length under the contact $L_T \ll D$, we have

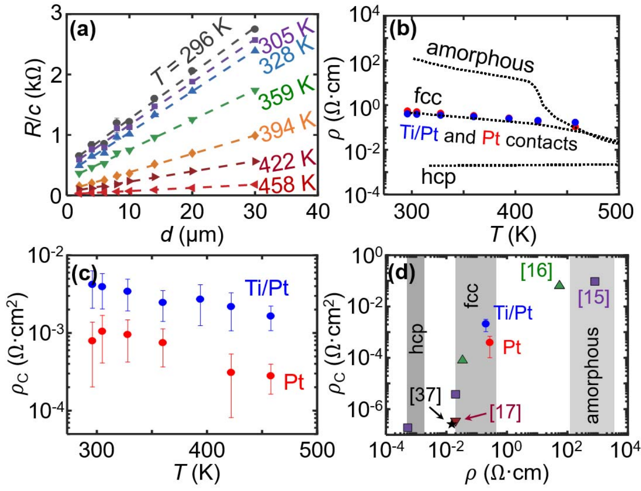

Fig. 2. C-TLM measurements of GST films. (a) Measured GST resistance with Ti/Pt contacts, corrected for circular geometry by factor c. Dashed line: linear fits for measured data. Smallest R-squared across all data was 0.989. (b) Extracted resistivity (ρ) with both Ti/Pt and pure Pt contacts (filled circles) versus temperature T, in agreement with cubic (fcc) GST from [23]; amorphous and hexagonal (hcp) GSTs shown (dotted lines) for comparison. (c) Extracted contact resistivity ρ_C versus T for our Ti/Pt and Pt contacts, with 90% confidence intervals. (d) Extracted ρ_C versus ρ for GST, from this study (blue and red circles) and from previous work, at RT. Gray bands represent typical ρ at RT [22], [23] for the various phases, and our ρ corresponds to fcc-GST. Previous studies are with TiW contacts (squares [15]), TiN (green [16] and maroon triangles [17]), and unspecified contacts (star [37]).

$A \approx \pi D L_T$ and $L_T \approx (\rho_C t_m/\rho)^{1/2}$. Combining these with (1), we obtain the final form of our C-TLM resistance equation as

$$\frac{R}{c} = \frac{\rho}{t_m}\frac{d}{\pi D} + \frac{2}{\pi D}\sqrt{\frac{\rho_C \rho}{t_m}}. \tag{2}$$

From one C-TLM measurement with Ti/Pt and Pt contacts each, the geometry-corrected resistance is shown in Fig. 2(a) where the resistance depends linearly on the electrode spacing d, as expected from (2). We also note that the resistance for the same electrode spacing decreases with increasing temperature up to 458 K, indicating enhanced thermionic emission at contact barriers and increased conduction in the semiconducting GST with higher temperature. Our extracted L_T are in the range of few 100 nm to few micrometers, which confirms our assumption $L_T \ll D$.

The extracted resistivity and the ρ_C of the GST film are shown in Fig. 2(b) and (c), respectively. The fcc state of the GST is confirmed by the match between the extracted resistivity and the temperature-dependent resistivity for GST reported elsewhere [22], [23] over all measured temperatures. The extracted ρ_C in Fig. 2(c) decreases with increasing ambient temperature and is independent of the current. Thermionic emission over and field emission through a Schottky barrier show a similar temperature dependence [24]. No significant polarity dependence of the current was observed, due to the symmetric nature of the test structure. Fig. 2(d) shows that lower ρ_C values could be obtained [17] for metal-nitride contacts with GST films of lower resistivity ρ, e.g., in the hcp phase or a mixture of the fcc and hcp phases. However, possible effects from GST film surface oxidation cannot be ruled out in our measurements. In our case, fcc-GST with Pt contacts yields lower ρ_C than with Ti/Pt contacts, probably due to a stronger reaction of Ti than Pt with the GST [25], [26], and the larger work function of Pt being better suited for the p-type GST.

B. L-TLM on TiO_2 Films

We measured temperature-dependent electrical characteristics for the L-TLM structures on TiO_2 shown in the inset of Figs. 1(c) and 3(a). The measured two-probe resistance for each adjacent pair of contacts is given by

$$R = \frac{\rho L_{\text{ch}}}{t_m W} + \frac{2\rho_C}{A} \tag{3}$$

where L_{ch} is the channel spacing, t_m is the film thickness, W (= 5 μm) is the contact width, and A is the effective contact area. The contact spacing varies between $L_{\text{ch}} \approx 30$ and 400 nm and the contact length $L_C = 0.5$ μm. Fig. 3(a) shows measured current versus voltage (I–V) data for the L-TLM structures at RT. The current is sub-4 pA at RT and increases to above 1 nA at 458 K. The measured, temperature-dependent resistance (at a constant current for each T) for two sets of samples is shown in Fig. 3(b). We assumed $A \approx L_C W$ because the transfer lengths [x-intercepts in Fig. 3(b)] are greater than L_C. Devices display contact-dominated conduction at all temperatures and low (< 0.4 V) bias voltages; hence, the L-TLM plot has a weak dependence on L_{ch}. Devices become more conducting due to improved thermionic emission at a higher temperature. This dependence is reflected in the extracted ρ_C values shown in Fig. 3(c). The trend is reversible with respect to temperature, indicating that the increased conductivity is not due to a permanent change in the film morphology or contacts.

C. V-TLM on HfO_2 Films

We use vertical crossbar devices, shown in Fig. 4(a) [corresponding optical image in Fig. 1(d)] with varying HfO_2 thicknesses t_m, as V-TLMs. The measured I–V data for devices with three different t_m (= 7.5, 10, and 12.5 nm) are shown in Fig. 4(b). We see that the current increases with decreasing thickness and with increasing temperature. Bulk- and interface-dominated conductions both typically show a similar behavior [27] for materials with non-Ohmic conduction. This indicates the challenge in separating the contribution from contacts. Although the temperature dependence is inconclusive about the dominance of interface versus bulk conduction, we perform a TLM-like extraction, which yields an average contact resistivity ($\rho_{\text{C,eff}}$) dependent on current density ($J = I/A$)

$$\rho_{\text{C,eff}}(J) = \lim_{t_m \to 0} \frac{V}{2J}. \tag{4}$$

To perform this estimate, we look at I–V data points corresponding to a similar range of device current. The area of all devices measured is $A = 48$ μm^2 with a large surface-to-perimeter ratio. We thus assume an average current density over the crossbar area. Fig. 4(c) shows that when plotted at different values of current, the resistance weakly scales with the thicknesses t_m of the HfO_2. The resistance also decreases

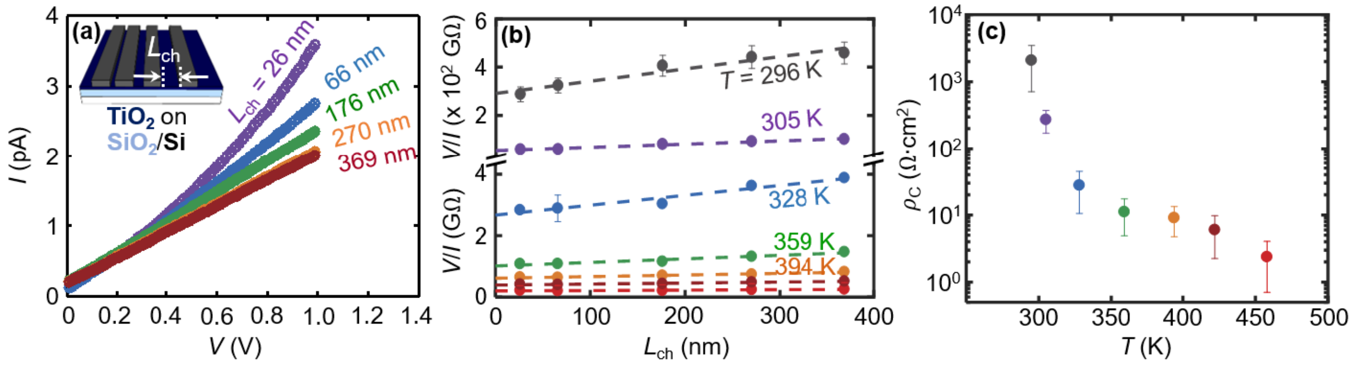

Fig. 3. L-TLM measurement of TiO_2 films. (a) Measured I–V for different channel lengths L_{ch} at RT (inset shows schematic of test structure). (b) Measured V/I versus L_{ch} at a constant current for several temperatures and two sample sets. Note split y-axis to show all data. Dashed lines are linear fits, with smallest R-squared of 0.855. (c) Corresponding extracted contact resistivity (ρ_C) for temperatures 296–458 K; error bars show 90% confidence intervals. Extracted resistivity ρ decreases from ~2 MΩ·cm to 0.6 kΩ·cm over this temperature range.

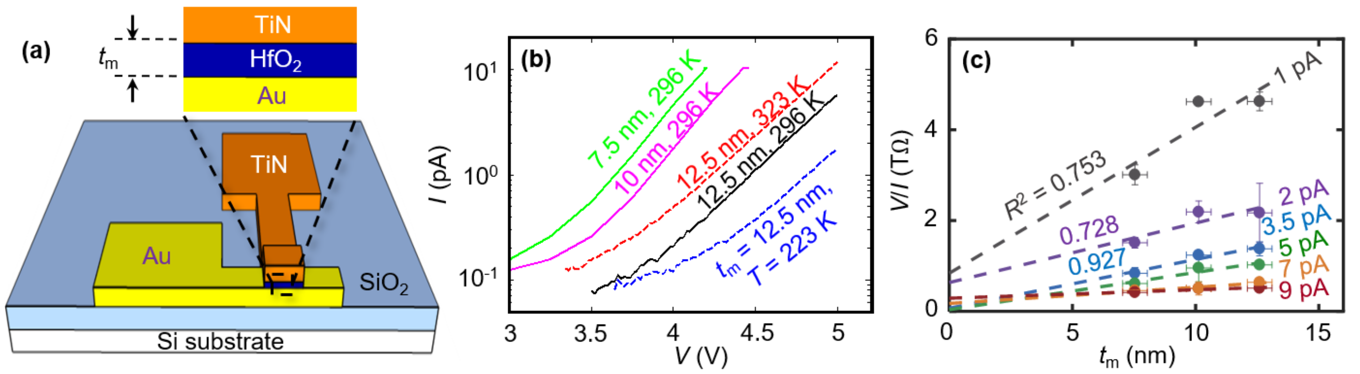

Fig. 4. V-TLM with HfO_2. (a) Schematic showing a typical crossbar device with oxide thickness t_m. (b) Measured I–V from crossbar devices with different oxide thicknesses at three different temperatures. (c) V-TLM fit as dashed lines to measured resistance at different current values, at RT. Values and vertical error bars are obtained from measuring three devices for each thickness. Horizontal error bars show the estimated variation of t_m from the standard deviation of HfO_2 thickness measured using ellipsometry. Goodness-of-fit R-squared values are shown for the first three fits; the lowest R-squared value for these data is 0.753.

with increasing device current. The slopes of the dashed lines correspond to an effective resistivity of 10^{13} to $6 \times 10^{13}\Omega\cdot$cm for the stoichiometric HfO_2 film, which is in the expected range of 10^{12}–$10^{14}\Omega\cdot$cm [28], [29]. The vertical intercepts of the linear fits in Fig. 4(c) are the effective contact resistance to the crossbar. Although the quality of this fit improves at higher current, we limit current density to prevent filamentation and damage in the HfO_2 film. A $\rho_{C,\text{eff}}$ of $10^5\Omega\cdot\text{cm}^2$ to $5 \times 10^5\Omega\cdot\text{cm}^2$ can be extracted from the vertical intercepts in Fig. 4(c), over all current values.

IV. Discussion

Contact resistivity versus temperature for different memory materials is shown in Fig. 5(a), compared with a few other known values. The ρ_C to GST in this work is lower than previously measured values to a-GST and higher than those to hcp-GST; a clear trend with the GST film resistivity is also shown in Fig. 2(d). While previous work on GST films employed cross-bridge Kelvin resistance (CBKR) measurements [15], our work across multiple material systems utilized C-TLMs, L-TLMs, and V-TLMs. ρ_C consistently decreases with increasing temperature, by up to two orders of magnitude over the plotted temperature range (≈0 °C to 200 °C), for each material system. The values of ρ_C for memory materials are several orders of magnitude higher than some of the lowest measured values for graphene [30], MoS_2 [21], Si [31], and other semiconductors. We note that while the energy band gaps of our measured films vary from ~0.5 eV (GST) [32] to ~5.4 eV (HfO_2) [33], the values of ρ_C vary over eight orders of magnitude in this work (and even more if the other data shown are included). This wide range of interfacial properties is an important consideration for scaling of both PCM and RRAM devices because contact resistance can dominate memory cell resistance depending on cell dimensions.

In Fig. 5(b), we plot contact resistance versus contact diameter for GST, TiO_2, and HfO_2 at RT along with measured PCM and RRAM total cell resistance (R_{total}). Contact resistance contributes to total-cell resistance significantly for GST-based PCM, both in the conducting and insulating states [6], [34]–[37], depending on the smaller contact diameter (typically the BE). These previously measured PCM cells exhibit a nonvolatile change in resistance similar to the change in ρ_C to fcc- and hcp-GST. On the other hand, our measured contact resistance to as-deposited oxides lies far above RRAM cell resistance values in both the low-resistance state (LRS) and the high-resistance state (HRS) down to sub-10-nm dimensions [38]–[41]. From Fig. 5(b), the LRS values measured in the literature for sub-10-nm HfO_2 (formed) RRAM filaments [38]–[41] indicate much lower contact resistance to the filament, possibly as low as the lowest

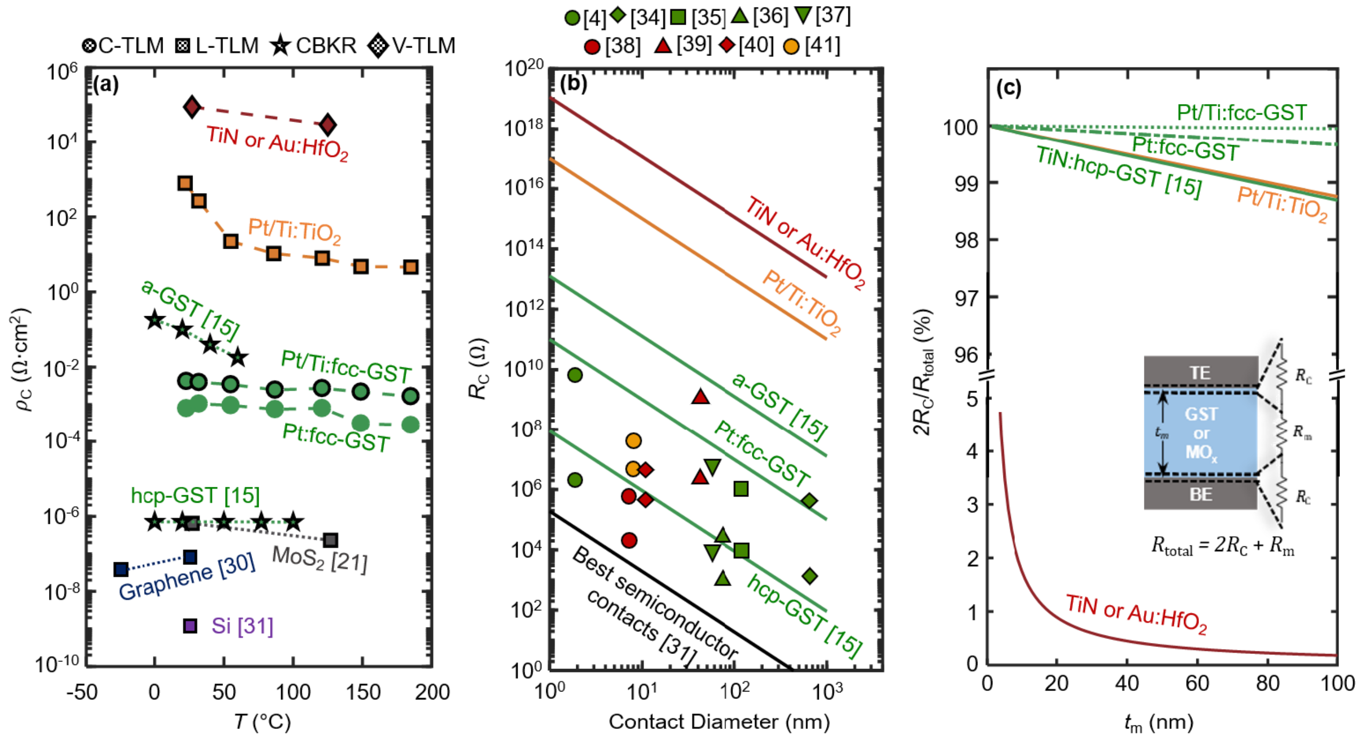

Fig. 5. (a) Contact resistivity (ρ_C) versus temperature (T): values shown for materials in this work (HfO_2, TiO_2, fcc-GST) and some of the lowest known values for other materials (Si, graphene, MoS_2, hcp-GST, a-GST). Symbol shape denotes test structure used: C-TLM (circle), L-TLM (square), V-TLM (diamond), and CBKR (star). Dotted and dashed lines are shown as guides for the eye. (b) Resistance versus contact diameter at RT: extracted and previously measured values from blanket films as lines; device total resistance values are plotted as symbols. Diameter considered is contact width for GST devices (green) and directly observed filament diameter for TiO_2 (orange) and HfO_2 (red) RRAM devices. (c) Estimated ratio of contact resistance to total cell resistance ($2R_C/R_{total}$) for a vertical device (inset) as a function of memory film thickness, t_m. Equal areas for top and bottom contacts are assumed. The ratios are calculated using contact resistivity and film resistivity values at RT.

demonstrated values of contact resistance to semiconductors ($\approx 1.5 \times 10^{-9} \Omega\cdot cm^2$ [31]). The HRS can have a contribution from ρ_C to HfO_x and TiO_x rich in oxygen vacancies, lower than the ρ_C to pristine HfO_2 and TiO_2, respectively.

Finally, we illustrate the contribution of contact resistance ($2R_C$) to R_{total} for memory cells based on our measured GST, TiO_2, and HfO_2 values, as shown in Fig. 5(c), as a function of film thickness, t_m. We note that pure Pt contacts to fcc-GST are better than those with 2-nm Ti/Pt due to a lower contribution to R_{total}. However, $2R_C$ dominates R_{total} over the t_m range considered for both GST and TiO_2. Thus, we see a need to improve ρ_C to GST in all three phases. For HfO_2, the intrinsic film resistivity appears to dominate R_{total}, except at sub-10-nm thickness for unformed films. However, the change in ρ_C after filament formation can contribute to device behavior in the LRS and remains an important parameter for future investigation. Our proposed V-TLM could be extended to the LRS and HRS in RRAM to extract contact and filament properties if the filament diameter and the gap thickness can be determined.

As PCM and RRAM store information in the resistance of the cell, estimating the contribution of contact resistance can reveal whether switching occurs at the interfaces or the bulk of the memory material. For PCM, high ρ_C indicates more Joule heating at the interface than in the PCM material bulk. Thus, alongside thermoelectric and heat-confinement considerations [34], controlling ρ_C provides an important means to reduce the PCM switching energy. For RRAM, if the ρ_C dominates, the device is more likely to switch at the filament–electrode interface, the LRS will be dominated by the higher contact resistance among the two interfaces, and the HRS will depend on the filament shape. If ρ_C is negligible, the device will switch mid-filament, while both the LRS and the HRS will be determined by the filament diameter at its narrowest point.

V. Conclusion

We measured and extracted the properties of three resistive memory materials (GST, TiO_2, and HfO_2) using three different contact resistivity test structures (C-TLM, L-TLM, and V-TLM) from 296 to 458 K. Within this temperature range, contact resistivity changes by up to two orders of magnitude for each material studied. This work is one of the first such low-current extractions done on pristine metal-oxide nonvolatile memory materials. We have also demonstrated an approach to extract contact resistivity from thin-film HfO_2, which is a non-Ohmic material. Here, we find that contact resistance to (unformed) HfO_2 is far larger than typical RRAM (LRS or HRS) cell resistance. On the other hand, for GST, we estimate from our measured contact and film resistivity values, that contact resistance can dominate PCM cell resistance. We expect that with the test structures and methodology demonstrated in this study, nonvolatile memories based on HfO_2, TiO_2, GST, and similar resistive switching

materials can be further optimized by improving corresponding contact resistances.

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References

[1] H.-S. P. Wong *et al.*, "Metal–oxide RRAM," *Proc. IEEE*, vol. 100, no. 6, pp. 1951–1970, Jun. 2012. doi: 10.1109/JPROC.2012.2190369.

[2] D. Ielmini, "Resistive switching memories based on metal oxides: Mechanisms, reliability and scaling," *Semicond. Sci. Technol.*, vol. 31, no. 6, May 2016, Art. no. 063002. doi: 10.1088/0268-1242/31/6/063002.

[3] S. Yu, *Resistive Random Access Memory (RRAM) : From Devices to Array Architectures*. San Rafael, CA, USA: Morgan & Claypool, 2016, pp. 1–79. doi: 10.2200/S00681ED1V01Y201510EET006.

[4] F. Xiong, A. D. Liao, D. Estrada, and E. Pop, "Low-power switching of phase-change materials with carbon nanotube electrodes," *Science*, vol. 332, pp. 568–570, Apr. 2011. doi: 10.1126/science.1201938.

[5] S. Raoux, F. Xiong, M. Wuttig, and E. Pop, "Phase change materials and phase change memory," *MRS Bull.*, vol. 39, pp. 703–710, Aug. 2014. doi: 10.1557/mrs.2014.139.

[6] F. Xiong *et al.*, "Towards ultimate scaling limits of phase-change memory," in *IEDM Tech. Dig.*, Dec. 2016, pp. 4.1.1–4.1.4. doi: 10.1109/IEDM.2016.7838342.

[7] Y. Huai, "Spin-transfer torque MRAM (STT-MRAM): Challenges and prospects," *AAPPS Bull.*, vol. 18, pp. 33–40, Dec. 2008.

[8] M. M. S. Aly *et al.*, "Energy-efficient abundant-data computing: The N3×T 1,000×," *Computer*, vol. 48, no. 12, pp. 24–33, Dec. 2015. doi: 10.1109/MC.2015.376.

[9] H.-S. P. Wong and S. Salahuddin, "Memory leads the way to better computing," *Nature Nanotechnol.*, vol. 10, pp. 191–194, Mar. 2015. doi: 10.1038/nnano.2015.29.

[10] C.-L. Tsai, F. Xiong, E. Pop, and M. Shim, "Resistive random access memory enabled by carbon nanotube crossbar electrodes," *ACS Nano*, vol. 7, no. 6, pp. 5360–5366, May 2013. doi: 10.1021/nn401212p.

[11] C. Ahn *et al.*, "Energy-efficient phase-change memory with graphene as a thermal barrier," *Nano Lett.*, vol. 15, no. 10, pp. 6809–6814, Aug. 2015. doi: 10.1021/acs.nanolett.5b02661.

[12] A. Padilla *et al.*, "Voltage polarity effects in $Ge_2Sb_2Te_5$-based phase change memory devices," *J. Appl. Phys.*, vol. 110, Sep. 2011, Art. no. 054501. doi: 10.1063/1.3626047.

[13] R. Waser and M. Aono, "Nanoionics-based resistive switching memories," *Nature Mater.*, vol. 6, pp. 833–840, Nov. 2007. doi: 10.1038/nmat2023.

[14] A. A. Sharma, I. V. Karpov, R. Kotlyar, J. Kwon, M. Skowronski, and J. A. Bain, "Dynamics of electroforming in binary metal oxide-based resistive switching memory," *J. Appl. Phys.*, vol. 118, Sep. 2015, Art. no. 114903. doi: 10.1063/1.4930051.

[15] D. Roy, M. A. A. I. Zandt, and R. A. M. Wolters, "Specific contact resistance of phase change materials to metal electrodes," *IEEE Electron Device Lett.*, vol. 31, pp. 1293–1295, Nov. 2010. doi: 10.1109/LED.2010.2066256.

[16] R. Huang *et al.*, "Contact resistance measurement of $Ge_2Sb_2Te_5$ phase change material to TiN electrode by spacer etched nanowire," *Semicond. Sci. Technol.*, vol. 29, Jul. 2014, Art. no. 095003. doi: 10.1088/0268-1242/29/9/095003.

[17] S. D. Savransky and I. V. Karpov, "Investigation of SET and RESET states resistance in ohmic regime for phase-change memory," *MRS Online Proc. Library Arch.*, vol. 1072, pp. 1–6, Feb. 2011. doi: 10.1557/PROC-1072-G06-09.

[18] D. O. Scanlon *et al.*, "Band alignment of rutile and anatase TiO_2," *Nature Mater.*, vol. 12, pp. 798–801, Jul. 2013. doi: 10.1038/nmat3697.

[19] F.-C. Chiu, "Interface characterization and carrier transportation in metal/HfO2/silicon structure," *J. Appl. Phys.*, vol. 100, Dec. 2006, Art. no. 114102. doi: 10.1063/1.2401657.

[20] J. H. Klootwijk and C. E. Timmering, "Merits and limitations of circular TLM structures for contact resistance determination for novel III-V HBTs," in *Proc. IEEE Int. Conf. Microelectron. Test Struct.*, Mar. 2004, pp. 247–252. doi: 10.1109/ICMTS.2004.1309489.

[21] C. D. English, G. Shine, V. E. Dorgan, K. C. Saraswat, and E. Pop, "Improved contacts to MoS_2 transistors by ultra-high vacuum metal deposition," *Nano Lett.*, vol. 16, no. 6, pp. 3824–3830, May 2016. doi: 10.1021/acs.nanolett.6b01309.

[22] B.-S. Lee, J. R. Abelson, S. G. Bishop, D.-H. Kang, B.-K. Cheong, and K.-B. Kim, "Investigation of the optical and electronic properties of $Ge_2Sb_2Te_5$ phase change material in its amorphous, cubic, and hexagonal phases," *J. Appl. Phys.*, vol. 97, Apr. 2005, Art. no. 093509. doi: 10.1063/1.1884248.

[23] K. Cil *et al.*, "Electrical resistivity of liquid $Ge_2Sb_2Te_5$ based on thin-film and nanoscale device measurements," *IEEE Trans. Electron Devices*, vol. 60, no. 1, pp. 433–437, Jan. 2013. doi: 10.1109/TED.2012.2228273.

[24] E. H. Rhoderick and R. H. Williams, *Metal-Semiconductor Contacts*, 2nd ed. Oxford, U.K.: Clarendon Press, 1988.

[25] V. A. Venugopal, G. Ottaviani, C. Bresolin, D. Erbetta, A. Modelli, and E. Varesi, "Thermal stability of $Ge_2Sb_2Te_5$ in contact with Ti and TiN," *J. Electron. Mater.*, vol. 38, no. 10, pp. 2063–2068, Oct. 2009. doi: 10.1007/s11664-009-0856-6.

[26] Q. Z. Hong and J. W. Mayer, "Thermal reaction between Pt thin films and Si_xGe_{1-x} alloys," *J. Appl. Phys.*, vol. 66, pp. 611–615, Aug. 1998. doi: 10.1063/1.343526.

[27] F.-C. Chiu, "A review on conduction mechanisms in dielectric films," *Adv. Mat. Sci. Eng.*, vol. 2014, Feb. 2014, Art. no. 578168. doi: 10.1155/2014/578168.

[28] E. Hildebrandt, J. Kurian, M. M. Müller, T. Schroeder, H.-J. Kleebe, and L. Alff, "Controlled oxygen vacancy induced P-type conductivity in HfO_{2-x} thin films," *Appl. Phys. Lett.*, vol. 99, Sep. 2011, Art. no. 112902. doi: 10.1063/1.3637603.

[29] F. M. Li *et al.*, "High-*k* (k=30) amorphous hafnium oxide films from high rate room temperature deposition," *Appl. Phys. Lett.*, vol. 98, Jun. 2011, Art. no. 252903. doi: 10.1063/1.3601487.

[30] H. Zhong *et al.*, "Realization of low contact resistance close to theoretical limit in graphene transistors," *Nano Res.*, vol. 8, no. 5, pp. 1669–1679, May 2015. doi: 10.1007/s12274-014-0656-z.

[31] H. Yu *et al.*, "1.5×10^{-9} Ωcm^2 contact resistivity on highly doped Si:P using Ge pre-amorphization and Ti silicidation," in *IEDM Tech. Dig.*, Dec. 2015, pp. 21.7.1–21.7.4. doi: 10.1109/IEDM.2015.7409753.

[32] T. Tsafack, E. Piccinini, B.-S. Lee, E. Pop, and M. Rudan, "Electronic, optical and thermal properties of the hexagonal and rocksalt-like $Ge_2Sb_2Te_5$ chalcogenide from first-principle calculations," *J. Appl. Phys.*, vol. 110, Sep. 2011, Art. no. 063716. doi: 10.1063/1.3639279.

[33] M. C. Cheynet, S. Pokrant, F. D. Tichelaar, and J.-L. Rouviere, "Crystal structure and band gap determination of HfO_2 thin films," *J. Appl. Phys.*, vol. 101, Mar. 2007, Art. no. 054101. doi: 10.1063/1.2697551.

[34] S. W. Fong, C. M. Neumann, E. Yalon, M. M. Rojo, E. Pop, and H.-S. P. Wong, "Dual-layer dielectric stack for thermally isolated low-energy phase-change memory," *IEEE Trans. Electron Devices*, vol. 64, no. 11, pp. 4496–4502, Nov. 2017. doi: 10.1109/TED.2017.2756071.

[35] D. Ielmini, A. L. Lacaita, A. Pirovano, F. Pellizzer, and R. Bez, "Analysis of phase distribution in phase-change nonvolatile memories," *IEEE Electron Device Lett.*, vol. 25, no. 7, pp. 507–509, Jul. 2004. doi: 10.1109/LED.2004.831219.

[36] A. Redaelli, A. Pirovano, F. Pellizzer, A. L. Lacaita, D. Ielmini, and R. Bez, "Electronic switching effect and phase-change transition in chalcogenide materials," *IEEE Electron Device Lett.*, vol. 25, no. 10, pp. 684–686, Oct. 2004. doi: 10.1109/LED.2004.836032.

[37] D. L. Kencke *et al.*, "The role of interfaces in damascene phase-change memory," in *IEDM Tech. Dig.*, Dec. 2007, pp. 323–326. doi: 10.1109/IEDM.2007.4418936.

[38] U. Celano *et al.*, "Imaging the three-dimensional conductive channel in filamentary-based oxide resistive switching memory," *Nano Lett.*, vol. 15, pp. 7970–7975, Nov. 2015. doi: 10.1021/acs.nanolett.5b03078.

[39] U. Celano, Y. Yin Chen, D. J. Wouters, G. Groeseneken, M. Jurczak, and W. Vandervorst, "Filament observation in metal-oxide resistive switching devices," *Appl. Phys. Lett.*, vol. 102, Mar. 2013, Art. no. 121602. doi: 10.1063/1.4798525.

[40] B. Govoreanu *et al.*, "$10\times10nm^2$ Hf/HfO_x crossbar resistive RAM with excellent performance, reliability and low-energy operation," in *IEDM Tech. Dig.*, Dec. 2011, pp. 31.6.1–31.6.4. doi: 10.1109/IEDM.2011.6131652.

[41] D.-H. Kwon *et al.*, "Atomic structure of conducting nanofilaments in TiO_2 resistive switching memory," *Nature Nanotechnol.*, vol. 5, pp. 148–153, Jan. 2010. doi: 10.1038/nnano.2009.456.