MULTIPHYSICS MODELING AND IMPACT OF THERMAL BOUNDARY RESISTANCE IN PHASE CHANGE MEMORY DEVICES

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ABSTRACT

Among the many emerging non-volatile memory technologies, chalcogenide (i.e. GeSbTe/GST) based phase change random access memory (PRAM) has shown particular promise. While accurate simulations are required for reducing programming current and enabling higher integration density, many challenges remain for improved simulation of PRAM cell operation including nanoscale thermal conduction and phase change. This work simulates the fully coupled electrical and thermal transport and phase change in 2D PRAM geometries, with specific attention to the impact of thermal boundary resistance between the GST and surrounding materials. For GST layer thicknesses between 25 and 75nm, the interface resistance reduces the predicted programming current and power by 31% and 53%, respectively, for a typical reset transition. The calculations also show the large sensitivity of programming voltage to the GST thermal conductivity. These results show the importance of temperature-dependent thermal properties of materials and interfaces in PRAM cells.

KEYWORDS: GST, GeSbTe, PRAM, thermal interface resistance, simulation

NOMENCLATURE

A_c	cross section area, m^2
A_s	area of side, m^2
C_{gst}	heat capacity, J/m^3K
C_p	specific heat capacity section area, J/kgK
ΔG^*	Gibbs energy, J
ΔH_f	enthalpy of formation, J
J	current density, A/m^2
L_c	diffusion length, m
T	temperature, K
Q'''	volumetric heat generation, J/m^3
Q_{dc}	Joule heat generation, J/m^3
R	resistance, Ω
R_{th}	thermal resistance, K/W
RC_{th}	thermal time constant, s
V	voltage, V
V_i	volume at interface, m^3
V_m	volume of a monomer, m^3
Z	acoustic impedance
d	thickness, m
dt_{max}	simulation time step, s
Δg	Gibbs energy per atom, J
k	thermal conductivity, $Wm^{-1}K^{-1}$
k_b	Boltzmann constant, J/K
q''	heat flux, W/m^2
r	radius, m
t	time, s
t_{AB}	transmission coefficient
w	heater radius, m

Greek Symbols

Δ_g	crystallization mesh size, m
α	thermal diffusivity, m^2/s
ϕ	electrical potential, V
γ	jump frequency, s^{-1}
η	viscosity, kg/m-s
θ	contact angle
ρ	density, kg/m^3
σ	electrical conductivity, $(\Omega\text{-m})^{-1}$
σ_s	surface energy, J/m^2
τ	thermal time constant, s
τ_s	nucleation time constant, s

INTRODUCTION

Demand for high density, reliable, and portable data storage has increased dramatically in recent years, leading to exploration of new technologies to overcome imminent challenges with current Flash based arrays. Phase change random access memory (PRAM) is a promising candidate for future non-volatile memory technologies due to its fast read/write characteristics and favorable scalability and endurance when compared with Flash technology [1]. Phase change random access memory (PRAM) devices use Joule heating during the application of a *programming current* to induce a transition between the crystalline and amorphous phases of a chalcogenide material such as GeSbTe (GST). The two phases have very different electrical conductivities, enabling the detection of the material state and information storage. The crystalline to amorphous programming transition, denoted as set to reset, is achieved by raising the GST above the melting temperature then rapidly quenching it before the molten region can recrystallize. The reset to set transition is achieved by heating the amorphous material above the glass temperature but below the melting temperature, accelerating the recrystallization process to times on the order of 100ns. Figure 1 illustrates these processes schematically.

Three important characteristics help distinguish PRAM from other emerging technologies: The amorphous and crystalline

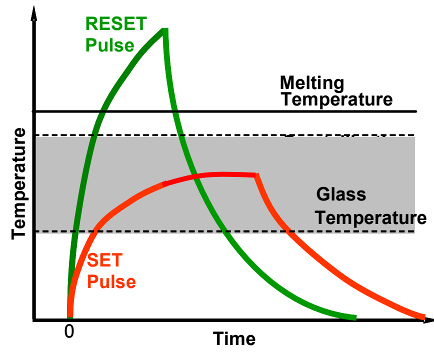

Fig.1 Schematic of the transitions between phases for a phase change memory device. Time scales are on the order of 10ns. The glass temperature is ~350°C and the melting temperature is ~650°C.

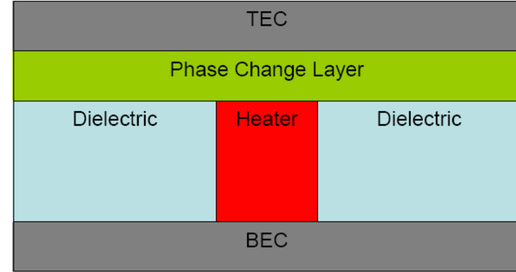

Fig.2 Standard PRAM cell design. Current enters through the bottom electrode (BEC), travels through the heater and phase change material (GST) layer and out the top electrode (TEC). Joule heating in the phase change layer induces reversible phase transformations between the amorphous and crystalline states of the material. The high and low resistivity of the two states, respectively, enables the memory function of the device.

phases are stable at room temperature, reduced dimensions lead to decreased programming currents, and device geometries are relatively simple, as illustrated in Figure 2. These features, respectively, allow for the device to meet the growing demand for non-volatile, scalable, low-cost memory [2]. Though attractive for these reasons, the simulation of PRAM devices requires accurate understanding of multiple physical processes including electrical and thermal transport and phase change. All of these processes are complicated by the small dimensions of the simulation domain. For example, typical dimensions of the standard cell in Figure 2 range from 65nm heater width to 50nm GST layer thickness. Heat conduction at these scales can be very strongly influenced by interface resistances, which become more important compared to volume resistances owing to the increasing surface to volume ratios inherent in nanostructures [3]. Accurate simulations are required for reducing programming current and enabling higher integration density, and many challenges remain for improved simulation of PRAM cell operation including nanoscale thermal conduction and phase change.

Previous simulations explored cell operation by examining scaling laws, thermal cross-talk between cells, resistance changes, electronic switching effects, and phase distribution. A detailed electronic model presented in reference [4] predicts the I-V behavior of amorphous and crystalline GST. This work describes the critical amorphous electronic switching effect: The transition from low to high electrical conductivity that permits the reset to set transition at low programming currents. Development of scaling laws and analysis of thermal cross-talk via simulation has been used to predict favorable scaling characteristics for PRAM devices [5]. Reference [6] links the set and reset phase distributions in the cell to experimental resistance data and calculated temperature profiles, emphasizing the importance of the temperature profile on predicting the phase distribution. While the past work emphasizes the importance of using detailed thermal and electrical properties and models, they have not accounted for the effects of thermal boundary resistance.

This work presents a comprehensive finite element (FE) simulation tool including phase change and the coupled electro-thermal physics accounting for thermal boundary resistances. Transient electro-thermal simulations incorporating thermal boundary resistance in FEMLab couple to a Matlab-based crystallization code to calculate temperature, voltage, and phase distributions. Using this tool we explore the impact of thermal boundary resistance at the GST interfaces on set to reset transitions and the sensitivity of cell peak temperature to thermal conductivity values.

This work enables more accurate simulation of the temperature fields in PRAM devices, in particular near the GST-metal interface. This work will therefore facilitate improved CAD of PRAM devices and eventually result reduced programming current and improved integration density.

PHYSICAL MODELING

The PCM device model consists of a thermal model for prediction of the transient temperature distribution in the device, an electrical model for predicting voltage and current distributions, and a crystallization model for simulating the behavior of the phase change layer. The thermal and electrical models are coupled via Joule heating and the combined electro-thermal model couples with the crystallization model via material property data.

Thermal model

Heat transfer phenomena are modeled using the transient heat equation with heat generation, Q_{dc},(= J^2/σ), temperature T, density ρ, specific heat C_p, and position and time dependent thermal conductivity, k, expressed as:

$$\nabla \cdot k(r,z,t)\nabla T + Q_{dc} = \rho C_p \frac{\partial T}{\partial t} \quad (1)$$

The temporal and spatial dependence of the thermal conductivity is applied only in the GST layer and results from the transient phase change process. The cell is modeled using axial symmetry with adiabatic boundaries, as shown in Figure 3. This study focuses on the impact of thermal interface resistance at the GST-metal and GST-dielectric contacts, and neglects other boundary resistances in the problem. Heat fluxes and temperature gradients at non-GST interfaces are

small relative to those at the GST interfaces, so the impact of the boundary resistance is negligible. As a consequence of these assumptions, temperature and energy continuity conditions apply at all internal boundaries not in contact with GST. Interfaces between the GST and surroundings incorporate a heat flux boundary condition to model the thermal boundary resistance. The condition at these interfaces may be written as:

$$q'' = \frac{\Delta T}{R_{th}} \qquad (2)$$

where q'' is the heat flux, R_{th} is the thermal boundary resistance on area basis in m^2K/W, and ΔT is the temperature difference across the interface.

Broadly accepted models of thermal boundary resistances at temperatures above tens of Kelvins do not currently exist. At temperatures below this, thermal boundary resistances result from a mismatch between two materials' speeds of sound and densities. Boundary resistances at these temperatures may be predicted with the acoustic mismatch (AM) model. This model assumes phonons are not scattered at the interface, yielding a transmission coefficient, $t_{AB} = 4Z_AZ_B/(Z_A+Z_B)^2$, where $Z=\rho c$ is the impedance defined in terms of the density, ρ, and speed of sound in the material, c. The partial transmission of phonons across the interface gives rise to the temperature discontinuity in equation 2 [7, 8]. To help explain boundary resistances at higher temperatures, Swartz proposed the diffuse mismatch model. This model assumes fully diffuse phonon scattering at the interface. The mismatch between the density of states of the two materials drives whether a phonon forward or backscatters, giving rise to a transmission probability that may be used to calculate the heat flux at the interface [8]. Both the AM and DM models provide insight into boundary resistances at and above room temperature, but neither captures the complex interaction between phonons and the surfaces necessary to provide confident estimates in room temperature interface resistance [7].

Experimental 3ω measurements for GST films show boundary resistances for amorphous and crystalline GST-ZnS:SiO_2 interfaces to be on the order of $2x10^{-8}$ and $0.6x10^{-8}$ Wm^2K^{-1}, respectively. The difference in boundary resistance is attributed to the acoustic properties of the different phases [9]. For reference, a boundary resistance of $2x10^{-8}$ m^2KW^{-1} is equivalent to the thermal resistance of ~20nm of silicon dioxide [7]. The thermal resistance of a 35nm crystalline GST layer is ~$7x10^{-8}$ Wm^2K^{-1}.

Because experimental data for the thermal boundary resistance is limited to GST-dielectric, the boundary resistance per unit area between the GST and surrounding materials is varied between 0 (i.e. perfect thermal contact) and $1x10^{-7}$ m^2KW^{-1}. This is a much larger range than typical room temperature boundary resistances for GST-dielectric and semiconductor-metal interfaces [7, 9]. It is chosen to accommodate realistic resistances at the lower end of the range and to demonstrate the impact of very large interface resistances.

Thermal conductivity values may be significantly altered from

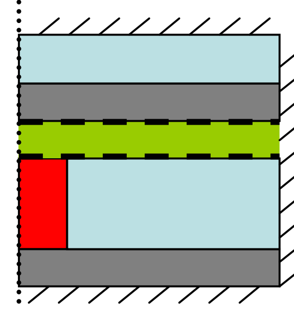

Fig.3 Thermal boundary conditions on the phase change memory cell. Dashed lines at the GST interfaces indicate a heat flux boundary condition is used to model the thermal boundary resistance.

their bulk due to their dependence on the microstructure of the thin films such as grain size, grain boundaries, structural anisotropy, defects, impurities, voids and interfaces [10]. Studies in optical phase change media show modified thermal conductivity values and inclusion of thermal boundary resistances are essential in reproducing accurate temperature profiles on length scales similar to those in PCM devices [11]. These effects are accounted for where possible. The temperature dependence of the thermal conductivities is neglected. Because device operation is over a very large temperature range (~300-1000K) the effects of this variation may be very significant, but no simple model or experimental data exists to address these variations. Instead a bi-valued thermal conductivity is used, one value for the crystalline and one value for the amorphous state, as cited in Table 1 [5]. Lastly, it is assumed latent heats associated with the solid-molten and molten-solid phase transitions are small compared to the energy associated with Joule heating and that associated with the thermal capacity of the materials at the melting temperature.

Electrical Model

Electrical phenomena in the device are modeled via a simplified version of Poisson's equation:

$$\nabla \cdot \sigma(r,z,t,E)\nabla\phi = 0 \qquad (3)$$

The electrical conductivity, σ, in the GST is a function of the crystalline state, which changes with time, t, and position, r and z, and, for amorphous GST, the local electric field E. It is assumed to be constant in the remaining material layers. Insulation boundary conditions are applied on all exterior boundaries except across the electrodes, where a constant voltage is applied. Continuity is applied at interior boundaries.

For the case of the set to reset simulations presented in this work, it is assumed up front the device has undergone electrical switching, the process whereby the amorphous phase change material enters a high conductivity state, assumed here to be equal to the crystalline conductivity, when exposed to an electric field above a certain threshold. This process, illustrated in Figure 4, is described in detail in [4]. Under this assumption, the GST electrical conductivity remains constant during the transition. Detection of the electrical resistance takes place at a voltage well below that required to switch the device, in which case the amorphous GST retains its low

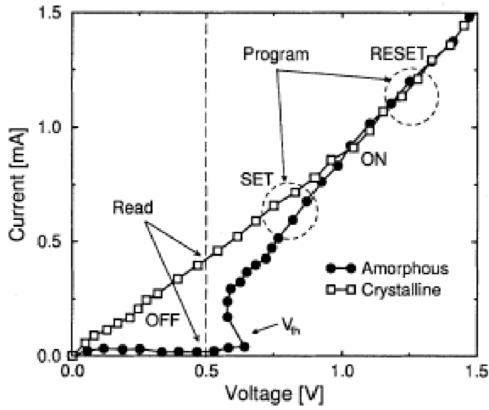

Fig.4 Experimental results for switching behavior in GST films in [4].

conductivity. Table 1 summarizes the thermal and electrical properties used in this work.

Table 1. Thermal and Electrical Material Properties [5, 10]

	k (W/mK)	C (J/m^3K)	σ $(\Omega\text{-m})^{-1}$
Al (electrodes)	25	2.45×10^6	$37 \times 10^{6*}$
GST-amorph./-molten	.17	1.25×10^6	3
GST-cryst.	.5	1.25×10^6	2770
Ti Alloy (heater)	17*	$7 \times 10^{5*}$	$1.12 \times 10^{5*}$
SiO2 (dielectric)	1.4	3.1×10^6	1×10^{-16}

* - bulk property

Crystallization Model

The crystallization model is based on classical nucleation and growth theory, as outlined in reference [12]. Though reference [12] indicates that there is no way to mathematically combine nucleation and growth into a single system of equations, the use of finite element model allows de-coupling of the two processes. In our simulation tool, the probability of nucleation is determined in one time step and the growth of nuclei is determined in subsequent steps.

Specifically, the model used is developed in [12]. The steady-state nucleation rate per unit volume is determined to be

$$I^{ss} = \frac{4\gamma}{V_m} n_c^{2/3} \sqrt{\frac{\Delta g}{6\pi n_c k_B T}} \exp\left[\frac{-\Delta G^*}{k_B T}\right] \qquad (4)$$

where γ is the molecular jump frequency, n_c is the number of molecules in a critical nucleus, V_m is the molecular volume, T is the temperature, Δg is the formation free energy difference per molecule, k_b is the Boltzmann constant, and ΔG^* is the energy barrier for nucleation. Table 2 lists the parameters and expressions used in equation 4.

The range of values for ΔH_f comes from differential scanning calorimetry experiments, and the expression for viscosity is estimated based on viscosity data for GeTe and incubation time experiments for GST [12]. The nucleation rate is particularly sensitive to variations in ΔH_f. Figure 5 shows the

Table 2. Crystallization Parameters and Expressions [12]

V_m [cm^3]	2.9×10^{-22}
σ_s [J/m^2]	.1
n_c [molecules]	$\frac{32\pi}{3}\frac{V_m^2\sigma^3}{\Delta g^3}$
ΔH_f [J/cm^3] (Enthalpy of Fusion at T_m)	610-625
T_m [K] (GST Melting Temperature)	900
Δg [J]	$\Delta H_f V_m \frac{T_m - T}{T_m}\left[\frac{7T}{T_m + 6T}\right]$
ΔG^* [J]	$\frac{16\pi}{3}\frac{V_m^2\sigma^3}{\Delta g^2}$
η [kg/(m-s)] (GST viscosity)	$1.94 x 10^{-14} \exp(\frac{2 \pm 0.1eV}{k_b T})$
λ [m] (jump distance)	2.99×10^{-10}
γ [s^{-1}]	$\frac{k_b T}{3\pi\lambda^3\eta}$

steady state nucleation rate as a function of temperature for various values of ΔH_f. Peak probabilities range from ~2×10^5 to 1.6×10^6 $cm^{-3}s^{-1}$.

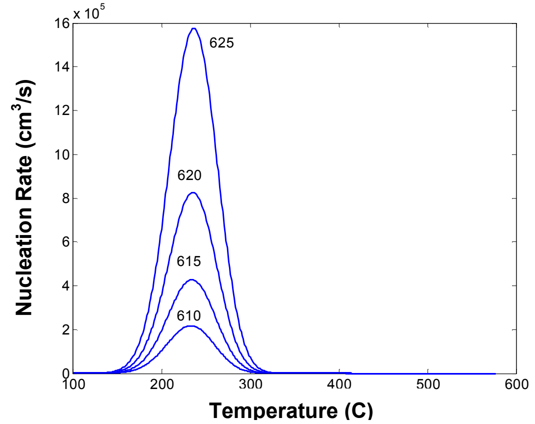

Fig.5 Steady state nucleation rate as a function of temperature for reported range of ΔH_f [12].

Transient effects are then dealt with by using the approach of Kashchiev [13],

$$I^{trans} = I^{ss}\left(\frac{4\pi\tau_S}{t}\right)^{1/2} \exp\left(\frac{-\pi^2\tau_s}{t}\right) \qquad (5)$$

where t is time and τ is defined as,

$$\tau_s = \frac{1}{\pi^3 n_c^{2/3} \gamma \frac{\Delta g}{6\pi n_c k_B T}}. \qquad (6)$$

Growth is determined by application of the method developed by Kelton and Greer [14], assuming a cluster has spherical geometry with radius r,

$$\frac{\partial r}{\partial t} = \frac{16 k_B T}{3\pi\lambda\eta}\left(\frac{3V_m}{4\pi}\right)^{1/3} \sinh\left[\frac{1}{2k_B T}\left(\Delta g - \frac{2\sigma}{r}V_m\right)\right]. \qquad (7)$$

Here, λ is the lattice constant, η is the viscosity (related to γ), and σ is the surface energy. Figure 6 illustrates the growth rates from this model. Kinetics parameters are in Table 2.

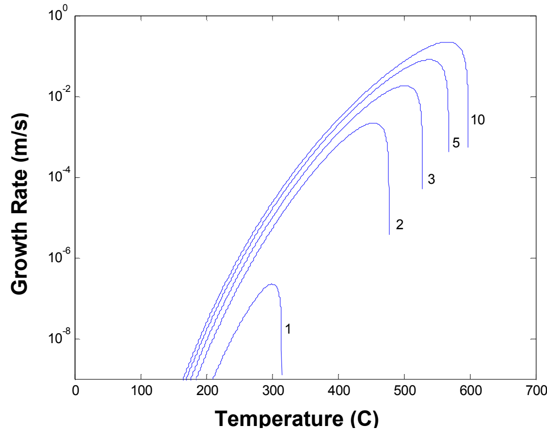

Fig.6 Growth rates as a function of temperature for various grain radii (in nm).

NUMERICAL IMPLEMENTATION

This model uses FEMLab Multiphysics to simulate the electrothermal interaction, calling the previously described crystallization code from Matlab to simulate the crystallization kinetics and update the material properties. FEMLab uses an internal loop with a controlled time step to satisfy the coupled electrical and thermal models. A simulation time step of dt_{max} is specified. After each simulation time step, FEMLab passes the temperature and electric field data from the most recently converged electro-thermal solution to the crystallization code in Matlab. The crystallization code interpolates the temperature and field data onto its own mesh and checks for melting, nucleation, and crystalline growth at each cell. Based on the updated crystalline status and electric field values, the code returns new thermal and electrical conductivity parameters to FEMLab. The process repeats after each dt_{max}, and is shown schematically in Figure 7.

As noted above, the crystallization code uses its own mesh and is called based on time steps defined by dt_{max}. The crystallization mesh is typically larger than the FE mesh used to solve the electro-thermal model because crystalline nuclei exist with a critical radius dependent on the local temperature. Below this radius, no stable crystalline nuclei exist. The crystallization code operates on a rectangular mesh with square elements $\Delta_g x \Delta_g$, where Δ_g =4nm is chosen as an average value of the critical radius for GST nuclei in the temperature range of interest (~600-900K). Similarly, the crystallization time step, dt_{max}=0.1ns, is defined taking into account the growth and nucleation models assume the region of interest is isothermal over a time step. Because rapid heating and cooling (~10^{11}K/s) are present in PRAM devices, the choice of dt_{max} represents a compromise between maintaining the isothermal assumption of the crystallization model and the time it takes to complete a simulation.

RESULTS and DISCUSSION

We performed 28 different set to reset simulations each with a unique combination of GST layer thickness and thermal interface resistance. The heater diameter in each simulation was 70nm and a constant voltage pulse was applied for 20ns. The voltage change across the cell varied in each simulation to

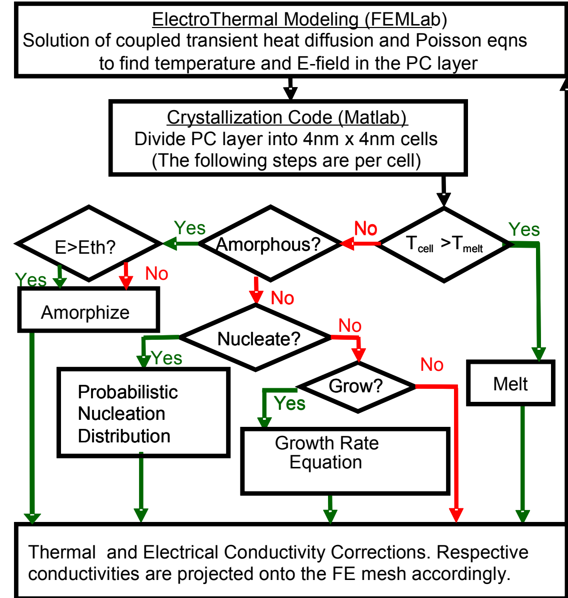

Fig.7 Schematic of numerical implementation

ensure the peak temperature in the cell stayed within the normal operating range of 1000-1050K. This allows a basis for comparison between simulations since, in general, it ensures set to reset resistance changes are similar. Additionally, cells exceeding this temperature range are prone to failure regardless of layer thickness and actual thermal interface resistance [1].

Resistance Change

Figure 8 shows the resistance change for each of the simulations. The unfilled set of points corresponds to the set resistance, while the filled points are resistance values after the set to reset transition. The set resistances in each case are approximately 2.1kΩ, while the typical reset resistances are 15-200% higher. The set values are consistent with experimental data reported in [1], [2], and [5]. The reset values are consistent with simulations in [6] for the case when the amorphous region does not fully cap the heater. In four simulations the amorphous region fully covered the heater. The readback resistance for these simulations was on the order of 500kΩ, consistent with experimental data in [1], [2], [4], and [5] and simulation data in [6].

The variations in reset resistances can be understood by examining the temperature profiles in Figures 9 a), b), and c). The cases with very large resistance result from the amorphous mark completely blocking the current path from the heater, as seen in Fig. 9a where the molten region clearly covers the entire heater. In this case, a series resistance forms between the heater, amorphous GST, crystalline GST, and top electrode. In the remaining cases, melting commences toward the middle of the GST layer and never fully encapsulates the heater, resulting in parallel electrical paths through the remaining crystalline GST and amorphous GST. This suggests the existence of two resistance regimes in the reset state, though the simulations do not offer a strong connection between the interface resistance and layer thickness with either regime.

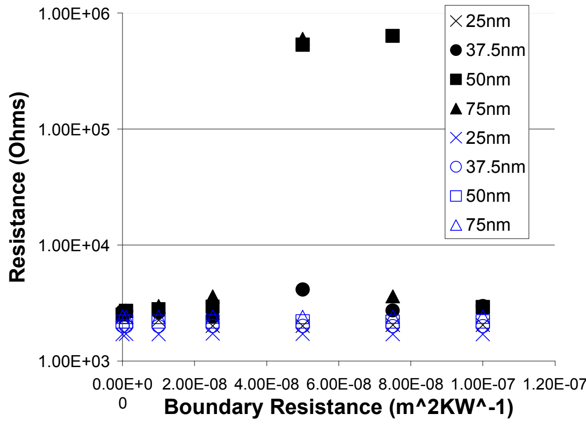

Fig.8 Predicted resistance in the set and reset states. The dashed vertical line indicates a cutoff above which the thermal boundary resistances are larger than one would likely dt_{max} encounter in practice.

The existence of two regimes can be explained by a simple heat diffusion argument. The location of melting onset is controlled by a competition between heat generation, proportional to the square of current density, and heat conduction away from the hot spot. Because the current spreads through the GST layer, the current density and hence heat generation rate decrease away from the heater interface, where it is at a maximum. However, thermal conduction is also near a maximum at the heater interface because the heater's thermal diffusivity is two orders of magnitude larger than that of GST. This effect is clear in Figure 9, which shows as conduction from the GST through the heater decreases (by including the interface resistance), the location of maximum temperature moves closer to the interface. Therefore, we would expect melting onset at the interface for cases when a high bias leads to large current densities and when a small heater diameter leads to both larger current densities for a given bias and decreased heat conduction.

The physical argument above can be quantified through a simple model based on energy conservation to a small region around the GST interface. This is illustrated schematically in Figure 10. For melting onset to occur at the interface, we require that the total energy generated in the volume minus the energy lost in the volume over a time τ exceeds the energy required to melt the material. This is expressed explicitly as:

$$\tau[Q'''V_i - (q''_{up} + q''_{down})A_c - q''_{side}A_s] > C_{gst}V_i\Delta T_m \tag{8}$$

where Q''' is a volumetric heat generation, q'' is a heat flux, V_i is the volume, A_c is the heater contact area, A_s is the lateral area of the volume, ΔT_m is the change in temperature required for melting, C_{gst} is the heat capacity per unit volume, and and τ is a characteristic time scale for melting.

By expressing $q''=\Delta T_m/R_{th}$, where $R_{th} = L_c/k$, where k is the thermal conductivity of the medium to which heat is being carried and L_c is a diffusion length over time τ in that material. With thermal diffusivity α we may rewrite (8) as:

$$\tau[Q'''V_i - (\frac{k_{gst}}{\sqrt{\alpha_{gst}\tau}} + \frac{k_{heater}}{\sqrt{\alpha_{heater}\tau}})A_c - \frac{k_{gst}}{\sqrt{\alpha_{gst}\tau}}A_s] > C_{gst}V_i\Delta T_m \tag{9}$$

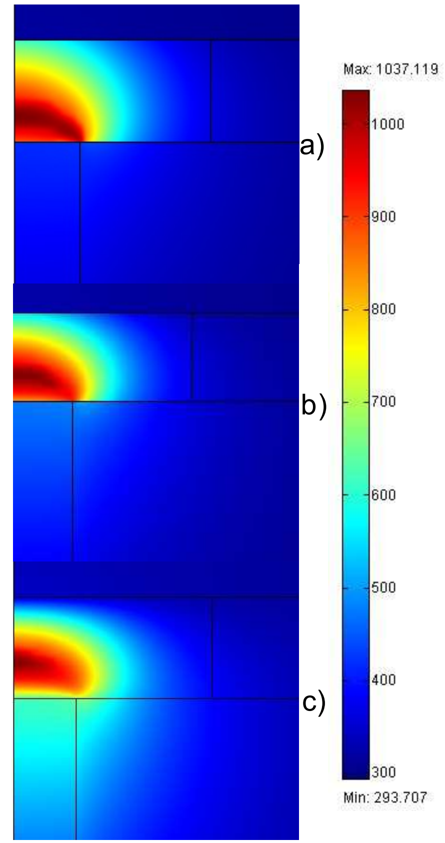

Fig.9 Temperature distributions showing the impact of interface resistance: **a)** 50nm GST layer with 5×10^{-8} m^2KW^{-1} thermal boundary resistance applied at the GST interfaces. **b)** 50nm GST layer with 2.5×10^{-8} m^2KW^{-1} resistance applied at the GST interfaces. **c)** GST layer with no interface resistance.

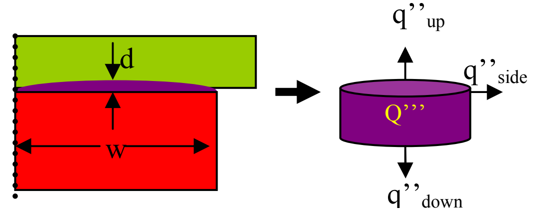

Fig.10 First Law applied to a small volume at the GST-heater interface.

At the interface, the volumetric heat generation is the square of the current density, J, divided by the electrical conductivity, σ (i.e. $Q''' = J^2/\sigma$). Substituting for J using Ohm's law and the given geometry at the interface,

$$Q''' = \frac{V^2}{R}\frac{1}{R\pi w^2\sigma} \tag{10}$$

where R is the set state resistance and V is the voltage drop across the GST. Upon inserting (10) and the geometry information into (9), the criterion for melting at the interface becomes:

$$\tau\left[\frac{V^2}{R}\frac{1}{R\pi^2w^4\sigma} - (\frac{k_{gst}}{\sqrt{\alpha_{gst}\tau}} + \frac{k_{heater}}{\sqrt{\alpha_{heater}\tau}})\frac{\Delta T_m}{d} - \frac{2k_{gst}}{\sqrt{\alpha_{gst}\tau}}\frac{\Delta T_m}{w}\right] > C_{gst}\Delta T_m \tag{11}$$

Figure 11 shows the results of this analysis for various values of w and V. The parameter d is set as 1nm, the approximate

size of the FE mesh, and thus the first detectable region in the simulations with $T>T_m$. τ is determined through $\tau=\Delta T_m/(RC)_{th}$ where $(RC)_{th}$ is the thermal time constant, approximately $2x10^{11}$ K/s, yielding τ=3ns.

The regime map captures the relevant melting physics, is in agreement with the simulations performed, and may be used as a general guideline for the melting/resistance regime at a given heater radius and voltage; however, as the model is derived from scaling rules, it should be noted the diffusion terms, τ, and d may all vary by multiplicative constants.

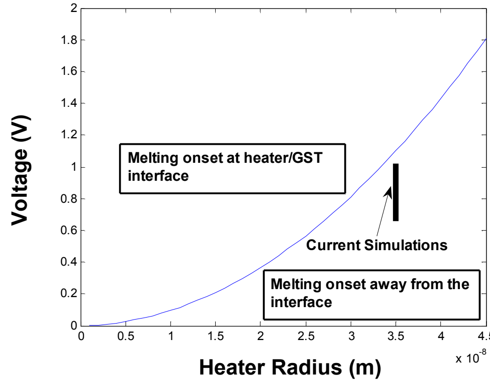

Fig.11 Regime map for melting onset location as a function of heater radius and voltage.

Set to Reset Sensitivity to k and Boundary Resistance

Seven simulations with constant thermal conductivity were performed on a GST layer thickness of 37.5nm with no thermal boundary resistance to determine the sensitivity of programming voltage to the crystalline GST thermal conductivity, k_c. The peak temperature for each simulation was 1030K. Figure 12 shows there is a drastic variation, from .69V to nearly 1.31V, in the programming voltage required to affect this temperature change for extreme values of k_c.

Intuitively, we expect an increase in required voltage for a given temperature rise/resistance change owing to increased thermal conductance within the GST. This effect is mediated, however, by an increase in the thermal diffusion length within the GST. Equation 11 shows this effect explicitly with two of the conductance terms proportional to $k_{gst}/\sqrt{\alpha_{gst}\tau}$.

The conductance within the GST is, thus, proportional to $\sqrt{k_{gst}}$. Since the temperature rise in the volume is dictated by the difference between the heat generation rate and the heat conduction rate, for a constant temperature rise we expect the V vs. k slope to level off as the V^2 term begins to dominate over the $\sqrt{k_{gst}}$ term. This is consistent with Figure 12.

The high sensitivity of programming voltage to the GST thermal conductivity suggests accurate simulations must incorporate both accurate thermal conductivity values and must adopt models that allow for varying thermal conductivities as the device changes state. Furthermore, as the thermal conductance of the GST layer increases, the thermal interface resistances play a significant role in determining the temperature profile and the programming voltage. Figure 12 shows that including a boundary resistance of $5x10^{-8}$ m^2KW^{-1} impacts the predicted programming voltage in roughly the same manner as halving the thermal conductivity. These results imply the need for accurate measurement of thermal conductivities and thermal interface resistances over a range of operating temperatures in the device.

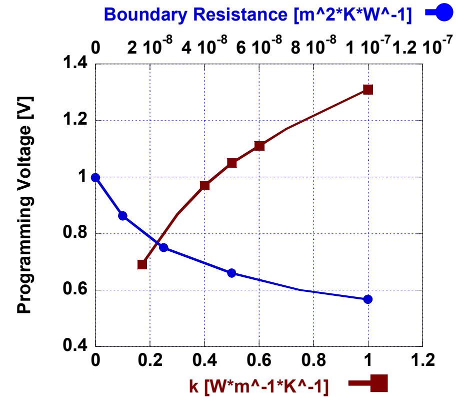

Fig.12 Sensitivity of the required voltage for set to reset transition on thermal conductivity and boundary resistance.

Programming Current and Power

Figures 13 and 14 show the dependence of programming current and power, respectively, on the thermal boundary resistance and layer thickness for the set to reset transition. It is clear from both figures that the presence of the thermal boundary resistance most significantly impacts thinner layers. The thin film thermal resistance is proportional to its thickness. Therefore as the layer thickness decreases, the thermal boundary resistance becomes increasingly important in the effective thermal resistance, which may be viewed as the series sum of the boundary and thin film resistances. As was previously discussed, this resistance (or conductance) dominates the thermal characteristics of the device.

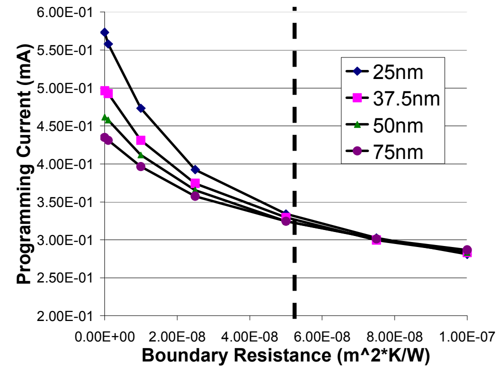

Fig.13 Impact of thermal boundary resistance on predicted programming current. The dashed vertical line indicates a cutoff above which the thermal boundary resistances are larger than one would encounter in practice.

Even for the thickest layer examined, the presence of $2.5x10^{-8}$ m^2KW^{-1} interface resistance per unit area, a reasonable value for this system, leads to reductions in predicted programming

current and power of 9% and 33%, respectively. In the thinnest layer, the same interface resistance caused reductions

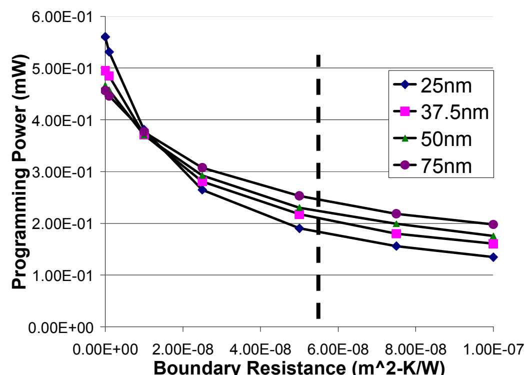

Fig.14 Impact of thermal boundary resistance on programming power in a set to reset transition. The dashed vertical line indicates a cutoff above which the thermal boundary resistances are larger than one would encounter in practice.

in programming current and power of 31% and 53%, respectively when compared with the zero boundary resistance case. Though, as indicated by Figure 8, the set to reset resistance change was generally unaffected by including the interface resistance, its presence carries the same significance as the intrinsic conductivity of the GST in terms of its effect on the predicted programming currents and power.

SUMMARY and CONCLUSION

This work presents a comprehensive finite element model used to explore the impact of thermal boundary resistance in phase change memory cells by simulating set to reset transitions for 28 unique combinations of boundary resistance and GST layer thickness. It is shown the presence of thermal boundary resistance in the simulation significantly impacts the temperature profile in the phase change layer.

For some combinations of layer thickness and thermal boundary resistance the modified temperature profile led to an amorphous ring or cap completely blocking the current path in the GST and leading to very large set to reset resistance changes consistent with experiments. The presence of boundary resistance was necessary to affect this resistance change. More often, an amorphous island was formed within the crystalline GST layer, leading to much smaller resistance changes between the set and reset states. An analytical regime map explains this phenomenon by viewing the location of melting onset as a trade off between heat conduction and Joule heating dependent on the heater diameter and the programming voltage/current.

A sensitivity study shows the intrinsic thermal conductivity of the phase change material strongly influences the voltage/current required for a typical resistance change in a set to reset transition. Due to this sensitivity, phase (i.e. amorphous or crystalline) and temperature varying thermal conductivities should be included in device simulations if possible. The temperature dependence of thermal conductivity is much needed and should be investigated in future work. The presence of the thermal boundary resistance also strongly influences the voltage/current required to produce a typical resistance change. Temperature dependent measurements of the thermal boundary resistances between GST and surrounding materials are another important avenue of future work. Because the intrinsic conductivity and thermal boundary resistances are individually significant in terms of their effect on prediction of programming current and power, and both strongly influence the temperature profile in the device, it is vital to include the most accurate models available when developing PRAM device simulations.

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