ACS APPLIED MATERIALS & INTERFACES

www.acsami.org

Research Article

Area-Selective Atomic Layer Deposition for Resistive Random-Access Memory Devices

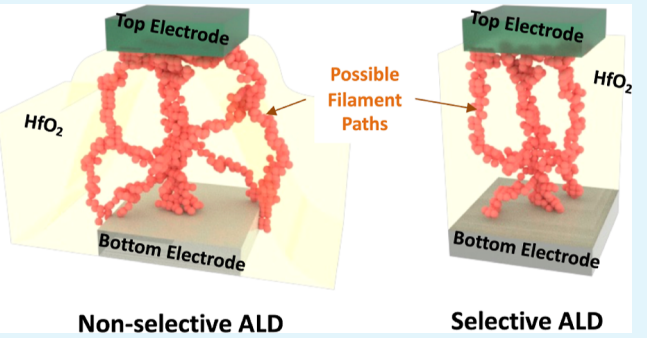
Il-Kwon Oh,*,⊥ Asir Intisar Khan,⊥ Shengjun Qin, Yujin Lee, H.-S. Philip Wong, Eric Pop, and Stacey F. Bent*

Cite This: *ACS Appl. Mater. Interfaces* 2023, 15, 43087−43093

Read Online

ACCESS | Metrics & More | Article Recommendations | Supporting Information

ABSTRACT: Resistive random-access memory (RRAM) is a promising technology for data storage and neuromorphic computing; however, cycle-to-cycle and device-to-device variability limits its widespread adoption and high-volume manufacturability. Improving the structural accuracy of RRAM devices during fabrication can reduce these variabilities by minimizing the filamentary randomness within a device. Here, we studied area-selective atomic layer deposition (AS-ALD) of the HfO_2 dielectric for the fabrication of RRAM devices with higher reliability and accuracy. Without requiring photolithography, first we demonstrated ALD of HfO_2 patterns uniformly and selectively on Pt bottom electrodes for RRAM but not on the underlying SiO_2/Si substrate. RRAM devices fabricated using AS-ALD showed significantly narrower operating voltage range (2.6 × improvement) and resistance states than control devices without AS-ALD, improving the overall reliability of RRAM. Irrespective of device size (1 × 1, 2 × 2, and 5 × 5 μm^2), we observed similar improvement, which is an inherent outcome of the AS-ALD technique. Our demonstration of AS-ALD for improved RRAM devices could further encourage the adoption of such techniques for other data storage technologies, including phase-change, magnetic, and ferroelectric RAM.



KEYWORDS: *area-selective atomic layer deposition, dielectrics, resistive random-access memory, filament confinement, data storage device*

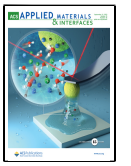
INTRODUCTION

Resistive random-access memory (RRAM) is one of the promising candidates for next generation nonvolatile memory and neuromorphic computing because of its excellent scalability, high speed, low power, and long endurance.[1−3] Typically in an RRAM device, a thin oxide layer such as HfO_2 is sandwiched between a bottom and a top electrode, and the memory states rely on charge conduction through the active oxide layer upon application of a voltage (or current) pulse. When there is a current-conducting path through the formation of a conductive filament between the two electrodes, the resistance of the device becomes low, whereas when the filament is broken, a high resistance state is realized.

A memory device needs to have uniform and repeatable cell characteristics to achieve high yield and reliability. However, RRAM devices face challenges with large variability and thus less reliability due to the random formation of filaments, which also cause fluctuations in the switching voltage.[4−9] This is aggravated by the process-induced randomness of the filament formation due to structural imprecision (e.g., the lack of a well-defined active device region)[1,10] during the conventional top-down fabrication process, which includes patterning.[11] For example, with the scaling down of devices, top-down fabrication faces the risk of edge placement error (EPE),[12,13] in which the overlay of unwanted material builds up, especially at the edge of the device. EPE can pose constraints on interdevice spacing, thus limiting the potential for higher-density memory.[14] Additionally, a top-down process has other problems, such as cost due to the large number of processing steps, a challenge that could otherwise be tackled using a bottom-up fabrication approach, such as area-selective atomic layer deposition (AS-ALD).

AS-ALD is a thin film deposition process that uses differences in surface reactivity to lead to the deposition of material onto desired regions of a substrate while avoiding deposition in other areas. It works by intentionally promoting or inhibiting the adsorption and nucleation of gas molecules on the surface, resulting in the selective growth of thin films in a specific area.[15−18] Thus, by using AS-ALD for atomic-scale growth control, the EPE can potentially be reduced. In addition, because AS-ALD enables mask-free patterning, it

Received: April 23, 2023
Accepted: August 1, 2023
Published: September 1, 2023



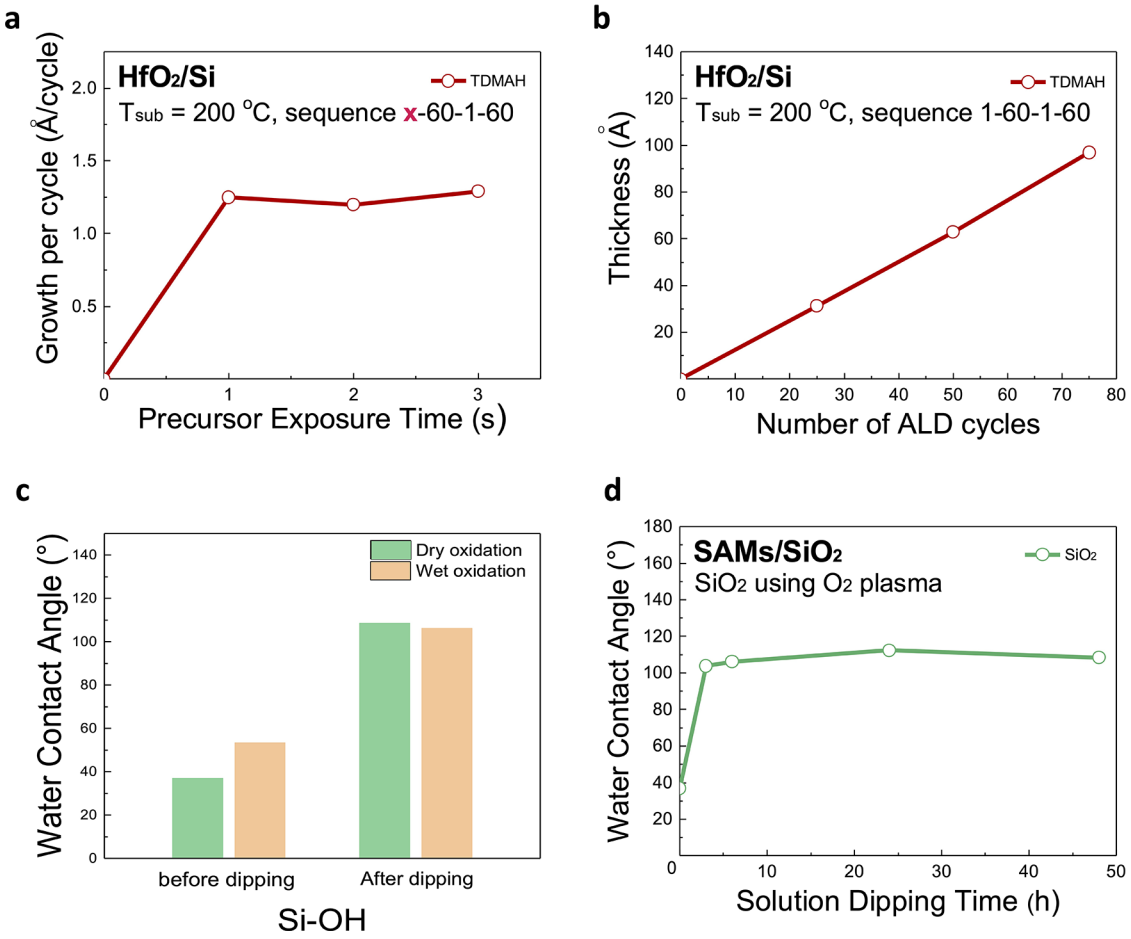


Figure 1. Growth characterization of area-selective ALD HfO_2. (a) Growth per cycle of HfO_2 on Si with SiO_2 native oxide as a function of precursor exposure. (b) Thickness of HfO_2 with the number of ALD cycles. (c) Water contact angle before and after ODTS solution dipping according to wet and dry treatment processes on SiO_2/Si. (d) Water contact angle with ODTS solution dipping time.

contributes to reduced complexity and a smaller number of lithographic exposure or etching steps.

In this work, we investigated the AS-ALD of HfO_2 dielectrics for the fabrication of RRAM devices. For the AS-ALD of HfO_2 (active material of the RRAM) patterns on Pt (bottom electrode), the SiO_2 surface regions of a Pt/SiO_2/Si substrate were selectively modified with inhibitors of self-assembled monolayers (SAMs), as confirmed by water contact angle (WCA) measurement, followed by HfO_2 ALD. The chemical composition and elemental mapping of HfO_2 were probed by Auger electron spectroscopy (AES), scanning electron microscopy (SEM), and X-ray photoelectron spectroscopy (XPS), further confirming the selectivity of HfO_2 deposition between Pt and SiO_2 substrates. RRAM devices were fabricated with AS-ALD HfO_2, and device performance was evaluated compared to those with nonselective ALD of HfO_2.

EXPERIMENTAL SECTION

Prior to SAM coating, the p-doped Si substrate was sonicated in acetone for 10 min, followed by 10 s in isopropanol to remove organic contaminants on the surface, and dried under flowing nitrogen. The sample was subsequently treated with either O_2 plasma (dry treatment) or H_2O (wet treatment) for 10 min under vacuum conditions of ~100 mTorr in an ALD reactor to produce a high concentration of surface hydroxyl groups. For patterned substrates used for RRAM devices, we first deposited 50 nm-thick Ti layers on the SiO_2/Si substrate for adhesion improvement below the bottom electrode material, Pt. Pt films of 100 nm in thickness were next electron-beam evaporated onto the Ti-coated SiO_2/Si substrate, followed by the definition of the patterns using a lift-off process. The patterning process includes the coating of the surface with photoresist, followed by optical photolithography and the subsequent development of the patterns. The deposited Ti/Pt metal films were then lifted off via solvent stripper to finalize the patterns. These patterned Pt/SiO_2 substrates were used for AS-ALD of HfO_2. After surface treatment, SAMs were coated on the Pt/SiO_2 patterns.

An octadecyltrichlorosilane (ODTS) SAM was used as an inhibitor for HfO_2 growth. The samples were immersed in a 1 mM solution of ODTS in toluene for 48 h at room temperature. After SAM coating, samples were sonicated for 10 min in toluene to remove physisorbed SAMs, followed by drying with N_2. The ODTS-coated substrates were transferred to ALD reactors for AS-ALD. We used two ALD reactors for HfO_2 AS-ALD: a custom reactor at Stanford University[19] was used for feasibility tests, and an Atomic Premium, CN1 Co. reactor at Ajou University was used for large-area demonstration. For the HfO_2 ALD processes, a tetrakisdimethylamino hafnium (TDMAH) precursor and deionized water counter reactant were pulsed at a growth temperature of 200 °C. The Hf precursor was held at 55 °C to maintain sufficient vapor pressure for delivery to the ALD reactor.

WCA goniometry measurement (SEO Co.) was performed to confirm SAM deposition. The chemical composition of the films on the surface was measured by XPS (ThermoFisher Scientific Co.). SEM (Physical Electronics Co.) and AES (Physical Electronics Co., PHI700) mappings were also conducted. The thickness and refractive index of the films were measured by spectroscopic ellipsometry (Ellipso technology Co.).

https://doi.org/10.1021/acsami.3c05822
ACS Appl. Mater. Interfaces 2023, 15, 43087−43093

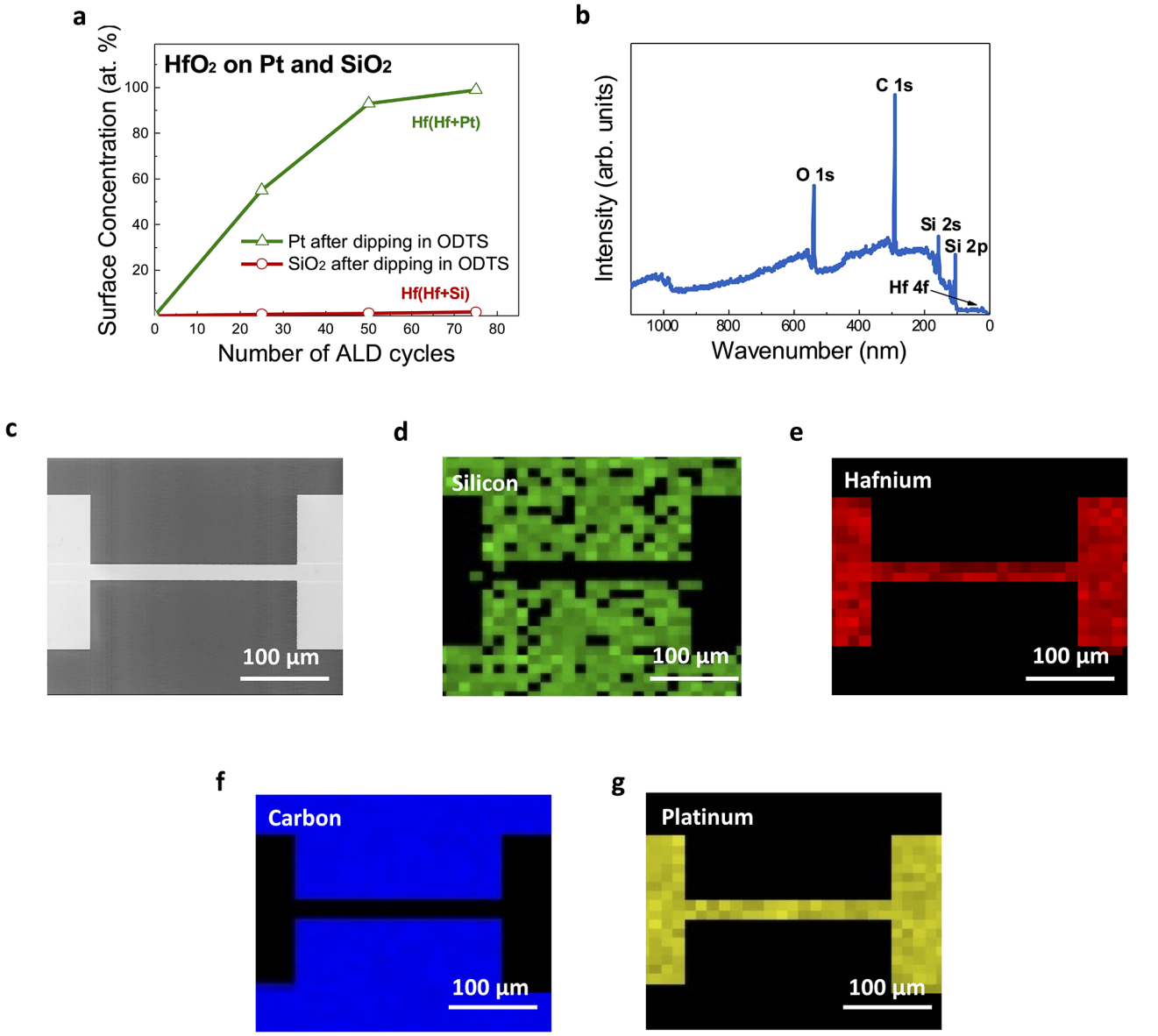


Figure 2. Material characterization. (a) Concentration of Hf measured by XPS; Hf/(Hf + Si) on SiO_2/Si; and Hf/(Hf + Pt) on Pt for HfO_2 ALD on SAM-coated substrates, which indicates the relative ratio of Hf on each surface. (b) XPS survey spectrum after 50 cycles of HfO_2 on SAM-coated SiO_2/Si showing no detectable Hf peaks. (c–g) SEM image and AES elemental mapping images of HfO_2 on SAM-coated Pt/SiO_2 patterns. (c) SEM image (bright: Pt and dark: SiO_2). Spatial AES images of (d) silicon (Si), (e) hafnium (Hf), (f) carbon (C), and (g) platinum (Pt) signals.

After selective ALD, the SAM was removed by 1 min of O_2 plasma exposure before depositing the top electrodes of the RRAM devices. TiN/Pt films with a thickness of 40 nm/20 nm were deposited (reactive sputtering of TiN and direct current (dc) sputtering of Pt) and defined by standard lift-off as the top electrodes. Thus, the fabricated RRAM devices were in a typical crossbar structure with a 5 nm-thick HfO_2 switching layer sandwiched between the metal electrodes. We also fabricated control HfO_2 RRAM devices by performing standard ALD of HfO_2, followed by patterning and etching to define the device region (no AS-ALD involved). The thickness of selective and uniform HfO_2 on Pt was measured by an ellipsometer, showing nearly the same results of about 5 nm. The fabrication process flow for the RRAM device with AS-ALD is presented in Figure S1 in the Supporting Information. The schematics of the fabricated RRAM devices are presented in Figure S2. Compared to a selective HfO_2 case (Figure S2a), uniform HfO_2 (Figure S2b) shows a larger program area. The reduced variability in our RRAM devices fabricated by using AS-ALD can be attributed to the better areal confinement of the HfO_2 switching region on the top of the bottom electrode compared to that for uniform ALD devices, enhancing the confinement and stability of filaments.

Electrical characteristics (current–voltage curves) of RRAM devices with and without AS-ALD HfO_2 were evaluated by using an Agilent B1500A Semiconductor parameter analyzer. The electrode sizes of the devices were varied between 1 × 1, 2 × 2, and 5 × 5 μm^2. Initially, the devices were in a high resistance state and needed to be activated with a forming process. A positive voltage was applied to the top electrode to switch the device to a low resistance state (LRS) or ON state, while a reverse biased voltage switched it back to a high resistance state (HRS) or OFF state.

RESULTS AND DISCUSSION

Figure 1a,b shows the growth characteristics of HfO_2 ALD using TDMAH and H_2O as the precursor and counter reactant, respectively. Figure 1a shows that the growth per cycle (GPC) gradually saturates at 1.3 Å/cycle as the precursor exposure time is increased. Therefore, the precursor undergoes

https://doi.org/10.1021/acsami.3c05822
ACS Appl. Mater. Interfaces 2023, 15, 43087–43093

a self-limiting reaction. Figure 1b shows that the thickness increases linearly as the number of ALD cycles increases, indicating the possibility of thickness control by adjusting the number of ALD cycles. Figure 1c,d shows the WCA values of the Si substrate with SiO_2 for different substrate treatment processes (dry and wet) and the SAM solution dipping time. A significant increase of WCA is observed after dipping the SiO_2 substrates, indicating hydrophobic SAM coating on the Si surface with SiO_2 (Figure 1c). These WCA values (above 100°) are comparable with previous reports on AS-ALD.[18,20] Both dry and wet treatments are effective in allowing inhibitor coating on SiO_2/Si, with a slight difference of WCA values. Figure 1d shows that the WCA values saturate with increasing solution dipping time for the SiO_2/Si substrate prepared by dry treatment. For the subsequent experiments, we chose 24 h to ensure sufficient coating of the SAM layers on the SiO_2/Si substrate made by dry treatment.

Figure 2a shows the relative concentration change of Hf on ODTS-SAM-coated Pt and SiO_2 substrates as the number of ALD cycles increases. Even after the SAM coating, the concentration of Hf gradually increases on a Pt substrate. The result indicates that SAM blocking is not effective for the Pt substrate, which we attribute to a low concentration on the Pt noble metal surface of O−H groups, which are needed for bonding to the SAM headgroup, leading to poor packing of the SAM on Pt.[17] This conclusion is consistent with WCA measurements showing almost no difference of WCA on Pt before and after SAM coating (58−60°) (data not shown).

On the other hand, the concentration of Hf remains nearly zero up to 75 cycles of HfO_2 ALD on a SAM-coated SiO_2/Si substrate. The result suggests that ODTS SAMs are packed well enough to block the adsorption of Hf precursor to the substrate, in agreement with the high WCA value shown in Figure 1c,d. The resulting selectivity of HfO_2 ALD to Pt over the SiO_2/Si substrate is in alignment with a previous report.[17] The calculated selectivity of HfO_2 on Pt versus SiO_2/Si is 97.5 and 96.6% at 50 and 75 cycles, respectively, estimated using $S_x = (R_{gs} - R_{ns})/(R_{gs} + R_{ns})$, where S_x is the selectivity after x ALD cycles, and R represents the atomic composition of the deposited material as a function of the substrate. Specifically, R_{gs} represents the atomic composition ratio of Hf/(Hf + Pt) for the growth surface (gs), and R_{ns} represents Hf/(Hf + Si) for the nongrowth surface (ns). Figure 2b shows an XPS survey spectrum after 50 cycles of HfO_2 ALD on ODTS-coated SiO_2/Si. No notable Hf peak can be seen, confirming that AS-ALD HfO_2 was successfully performed.

Figure 2c shows an SEM image of 5 nm-thick ALD-HfO_2 deposited on SAM-coated Pt/SiO_2 patterns. The dark region represents the SiO_2/Si substrate, whereas Pt is present in the light-colored regions. The same sample was used for elemental mapping analysis by AES, as shown in Figure 2d−g. Figure 2d−g confirms that the Hf signal is only detectable on the Pt areas of the pattern. Also, in Figure 2f, the carbon signal is observed principally in SiO_2/Si areas of the substrate and not on Pt, consistent with selective ODTS SAM formation on SiO_2/Si. In contrast, when HfO_2 ALD is performed without a SAM inhibitor on the same Pt/SiO_2 patterns, the Hf signal is detected across the entire substrate pattern, as shown in Supporting Information Figure S3, although we note that there is some inherent selectivity for growth on Pt observed even without the SAM (which could possibly arise from a catalytic effect of the Pt substrate[21]). Thus, with ODTS-assisted AS-ALD, HfO_2 films are successfully deposited only on Pt, a bottom electrode for the RRAM devices, and not on the SiO_2/Si substrate. Additionally, we compare the impurity content in both HfO_2 films by XPS because impurities such as carbon can degrade device performance (Figure S4 and Table S1 in the Supporting Information). The results show only a very small amount of carbon impurity for selective HfO_2 (~0.4%), and no carbon or nitrogen impurities in uniform HfO_2 with respect to the detection limits.

This technique is not limited to the fabrication of bottom electrodes for RRAM devices; rather, it can be readily used for fabricating the ultrascaled and precise bottom electrodes of other competing memory technologies such as phase-change RAM,[22] magnetic RAM,[23] and ferroelectric RAM.[24] In each case, since AS-ALD is based on the specific chemical reactions at the surface, it will be necessary to select an appropriate combination of inhibitor and precursor depending on the type of substrate and material to be deposited.

Figure 3a,b shows current (I) vs voltage (V) plots for RRAM devices (1 × 1 μm^2 active device regions) taken across 50

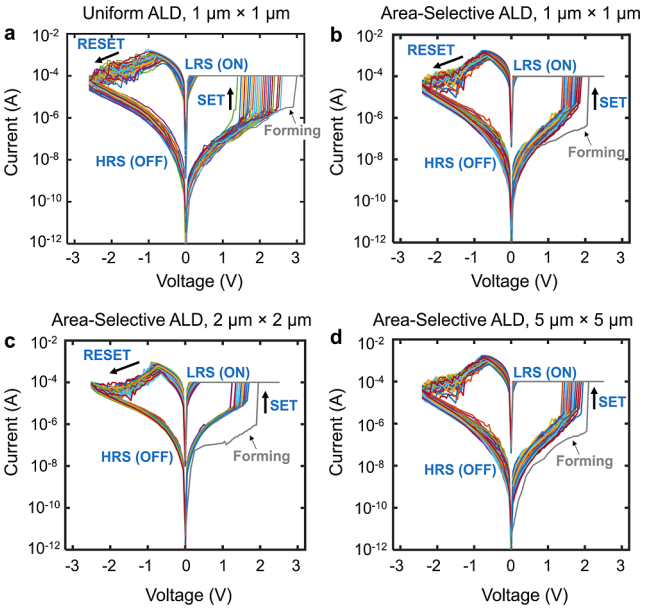


Figure 3. Electrical measurements of area-selective ALD RRAM devices. Current (I)−voltage (V) curves of RRAM devices depending on the fabrication method for HfO_2 of (a) uniform ALD with 1 × 1 μm^2, (b) area-selective ALD with 1 μm × 1 μm^2, (c) area-selective ALD with 2 × 2 μm^2. (d) Area-selective ALD with a 5 × 5 μm^2 active device region. Forming curves for each device are shown in gray.

consecutive cycles on RRAM with uniform (i.e., non-area-selective) and AS-ALD of HfO_2, respectively. The switching voltage of the AS-ALD RRAM devices shows a significant reduction in cycle-to-cycle variation compared to their nonselective counterparts, in which the HfO_2 was more uniformly grown on Pt/SiO_2 patterns. Considering the cycle-to-cycle variation, the SET voltage (the voltage at which the transition occurs from HRS to LRS) distribution in the selective ALD RRAM device shows a significantly narrower range (~0.5 V) compared to the nonselective design (~1.3 V), an improvement of ~2.6×. The reduced variability in our RRAM devices fabricated by using AS-ALD can be attributed to the better areal confinement of the HfO_2 switching region on top of the bottom electrode, thus enhancing the

https://doi.org/10.1021/acsami.3c05822
ACS Appl. Mater. Interfaces 2023, 15, 43087−43093

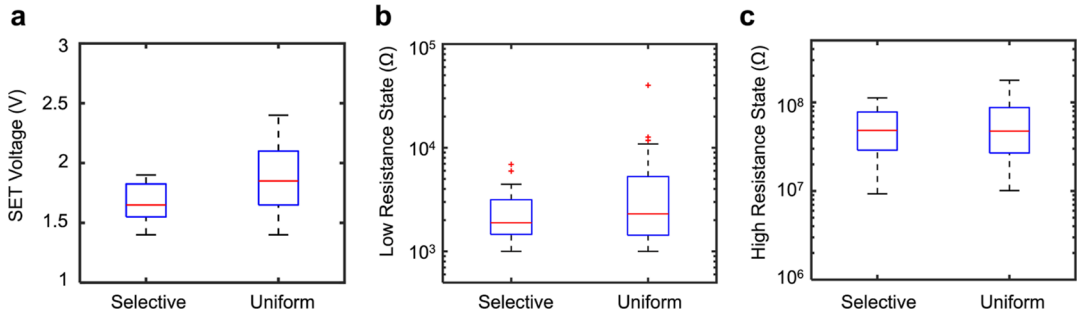


Figure 4. Distribution of (a) SET voltage, (b) low resistance state (LRS), and (c) high resistance state (HRS) comparing RRAM devices with selective-ALD and uniform ALD deposition methods. Fifteen different devices (and 25 DC switching cycles from each device) for both selective-ALD and uniform ALD depositions are included in the distribution. Compliance current for the measurements is 100 μA for all devices.

confinement and stability of filaments (as further detailed below).

A similar benefit for selective ALD RRAMs can also be discerned for the resistance distributions in the LRS and HRS, with a 280 and 292% reduction in the distribution variation, respectively, compared to the nonselective ALD devices. We further explored the applicability and consistency of the selective ALD deposition technique in different cell sizes of the RRAM devices. Figure 3b–d plots I vs V for area-selective-ALD RRAM devices of different sizes (1×1, 2×2, and 5×5 μm^2) each measured for 50 consecutive cycles, confirming the reproducibility of stable device operation as well as low cycle-to-cycle variation irrespective of the device dimension. I vs V data for ten different devices (Figures S5 and S6 in Supporting Information) show that device-to-device variability is also reasonably low for our selective-ALD RRAM devices, showing the proof-of-concept reliability of the AS-ALD technique for RRAM device fabrication. We further note that the design (e.g., geometry of the electrodes) and fabrication process flow could be further optimized for large arrays and reliable high-volume manufacturing of future ultrascaled RRAM devices.

Figure 4a–c summarizes the statistical variation of SET voltage, LRS, and HRS comparing our selective ALD and uniform ALD RRAM devices. The average SET voltage for selective ALD RRAM devices (15 devices and 25 switching cycles for each device) is 1.67 ± 0.16 V, whereas for uniform ALD devices (15 devices and 25 switching cycles for each device), the average SET voltage is 1.87 ± 0.27 V (Figure 4a). Thus, the standard deviation of SET voltage is 40% lower in selective ALD RRAM devices, compared to control uniform ALD devices. The interquartile ranges of the SET voltage for selective ALD and uniform ALD RRAM devices (across different cycles) are 0.28 and 0.45 V respectively, further underscoring the lower SET voltage variability in selective ALD RRAM devices. Figure 4b shows lower LRS variability in the selective ALD devices (~2.4 ± 1.3 kΩ, interquartile range ~1.7 kΩ) compared to the control uniform ALD devices (~4.5 ± 6.15 kΩ (skewed data distribution), interquartile range ~3.8 kΩ). The average HRS of our selective ALD RRAM devices is ~53 ± 30 MΩ (interquartile range ~48.9 MΩ), whereas for our unform ALD RRAM, the average HRS is ~61 ± 42.6 MΩ with an interquartile range of 60.5 MΩ (Figure 4c). Thus, we also estimate ~78 and ~28% smaller standard deviations in the low and high resistance states of our selective ALD RRAM devices, respectively, compared to the control devices without selective-ALD, improving the overall reliability of RRAM devices. The reset voltage (i.e., the stopping voltage) is similar for both selective ALD and uniform ALD RRAM devices.

The reduced variability in our RRAM devices fabricated using AS-ALD can be attributed to the better areal confinement of the HfO_2 switching region (i.e., confinement of the possible locations of the filaments[9,22,23] on top of the bottom electrode compared to that for uniform ALD devices, thus enhancing the confinement and stability of filaments (Figure S2). Figure S2b shows a conventional crossbar RRAM device with nonselective ALD HfO_2, demonstrating the possible formation paths of random filaments due to the extended presence of the HfO_2 active region beyond the size of the electrodes. In contrast, the oxygen vacancies inside filaments in an AS-ALD HfO_2 RRAM device would be physically confined to a smaller region compared to uniform ALD RRAM devices, as illustrated in Figure S2a, which can reduce the variability by negating excess conductivity during the electrical bias application.[24] This further renders filaments more controllable under the electrical field imposed by the electrodes compared to the nonselective case.

Previous studies on the device performance of RRAM showed a dependence on device size because the number density of formed filaments increases as the device size increases, making it hard to control device performance precisely.[25] In addition, the projected area of HfO_2 outside of the electrodes increases with the device area, therefore increasing the possible filament formation paths, which can introduce more variability.[5] In contrast, compared to a conventional top-down process, this size-insensitive phenomenon may be attributed to an inherent characteristic of the AS-ALD process. Namely, the patterned HfO_2 films grow vertically, directly following the underlying pattern of the growth substrate, such that patterning resolution (pattern size) should not be limited, ideally. This performance consistency independent of active device size further shows the promise of AS-ALD for future three-dimensional (3D) heterogeneous integration of ultrascaled multilayer RRAM technology with low variability and higher reliability. Similar to vertical NAND flash memory, the separation of the active insulator will be required for further scaling down of 3D structures, which cannot be achieved by a conventional top-down fabrication based on photolithography. Also, the AS-ALD process can be utilized multiple times, which enables the deposition of nanolaminate layers.

Even though we did not directly compare HfO_2 films patterned by photolithography, the expectation is that AS-ALD reduces EPE compared to a conventional patterning process by preventing material from depositing in unwanted areas.[26] As an outlook, the reduced EPE can be useful to mitigate interdevice interference and variations in a high-density array of RRAM

https://doi.org/10.1021/acsami.3c05822
ACS Appl. Mater. Interfaces 2023, 15, 43087–43093

(or any other relevant memory technology) with closely spaced devices. Thus, our results indicate the promise of the selective ALD technique for addressing the cycle-to-cycle and device-to-device variation in a high-density RRAM array with ultrascaled devices.

CONCLUSIONS

In summary, we studied the area-selective ALD of HfO_2 dielectrics as the active layer for RRAM devices. We developed an AS-ALD process for depositing HfO_2 uniformly and selectively on patterned Pt bottom electrodes on an underlying SiO_2/Si substrate. Using the developed process, RRAM devices were fabricated, and their electrical characteristics were systematically compared. The devices with AS-ALD show significantly lower variability in terms of SET voltages and resistance states compared to their nonselective counterparts. These findings demonstrate the promise of the AS-ALD technique for reliable and high-density RRAM with ultrascaled devices and should further encourage the adoption of AS-ALD for other emerging memristor technologies.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.3c05822.

Device fabrication process flow, schematics of fabricated RRAM devices, AES images of uniform HfO_2, impurity contents in HfO_2 films, atomic concentration, $I-V$ measurement of ten RRAM devices with 1×1 μm^2 in size, and $I-V$ measurement of an additional two RRAM devices with 2×2 μm^2 in size (PDF)

AUTHOR INFORMATION

Corresponding Authors

Il-Kwon Oh − *Department of Chemical Engineering, Stanford University, Stanford, California 94305, United States; Department of Electrical and Computer Engineering and Department of Intelligence Semiconductor Engineering, Ajou University, Suwon 16499, South Korea;* orcid.org/0000-0002-1266-3157; Email: ikoh@ajou.ac.kr

Stacey F. Bent − *Department of Chemical Engineering, Stanford University, Stanford, California 94305, United States;* orcid.org/0000-0002-1084-5336; Email: sbent@stanford.edu

Authors

Asir Intisar Khan − *Department of Electrical Engineering, Stanford University, Stanford, California 94305, United States;* orcid.org/0000-0003-4635-4667

Shengjun Qin − *Department of Electrical Engineering, Stanford University, Stanford, California 94305, United States*

Yujin Lee − *Department of Chemical Engineering, Stanford University, Stanford, California 94305, United States*

H.-S. Philip Wong − *Department of Electrical Engineering, Stanford University, Stanford, California 94305, United States*

Eric Pop − *Department of Electrical Engineering, Stanford University, Stanford, California 94305, United States;* orcid.org/0000-0003-0436-8534

Complete contact information is available at: https://pubs.acs.org/10.1021/acsami.3c05822

Author Contributions

[⊥]I-K.O. and A.I.K. contributed equally to this work.

Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

The area-selective atomic layer deposition development was supported in part by NEW LIMITS, a center in nCORE, a Semiconductor Research Corporation (SRC) program sponsored by NIST, through award no. 70NANB17H041. This work was partially supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIT) (nos. 2021R1F1A1063671 and 2021R1A4A1033155). E.P. and H.S.P.W. acknowledge support from the member companies of the Stanford Non-Volatile Memory Technology Research Initiative (NMTRI). A.I.K. acknowledges support from the Stanford Graduate Fellowship. The authors thank R. Islam for useful discussions at the initial phase of this work during its conceptualization. A.I.K. is thankful to M. Chen for the lab support.

REFERENCES

(1) Zahoor, F.; Azni Zulkifli, T. Z.; Khanday, F. A. Resistive Random Access Memory (RRAM): an Overview of Materials, Switching Mechanism, Performance, Multilevel Cell (mlc) Storage, Modeling, and Applications. *Nanoscale Res. Lett.* **2020**, *15*, 90.

(2) Waser, R.; Aono, M. Nanoionics-based resistive switching memories. *Nat. Mater.* **2007**, *6*, 833−840.

(3) Chen, A. Ionic memory technology. *Solid State Electrochemistry II; Electrodes, Interfaces and Ceramic Membranes*; Kharton, V. V., Ed.; Wiley, [S.l.]. Cap., 2011; Vol. *1*, pp 1−26.

(4) Guan, X.; Yu, S.; Wong, H.-S. P. On the Switching Parameter Variation of Metal-Oxide RRAM-Part I: Physical Modeling and Simulation Methodology. *IEEE Trans. Electron Devices* **2012**, *59*, 1172−1182.

(5) Yun, J.-B.; Kim, S.; Seo, S.; Lee, M.-J.; Kim, D.-C.; Ahn, S.-E.; Park, Y.; Kim, J.; Shin, H. Random and localized resistive switching observation in Pt/NiO/Pt. *Phys. Status Solidi RRL* **2007**, *1*, 280−282.

(6) Degraeve, R.; Fantini, A.; Raghavan, N.; Goux, L.; Clima, S.; Govoreanu, B.; Belmonte, A.; Linten, D.; Jurczak, M. Causes and consequences of the stochastic aspect of filamentary RRAM. *Microelectron. Eng.* **2015**, *147*, 171−175.

(7) Wu, E.; Ando, T.; Kim, Y.; Muralidhar, R.; Cartier, E.; Jamison, P.; Wang, M.; Narayanan, V., Filamentary Statistical Evolution from Nano-Conducting Path to Switching-Filament for Oxide-RRAM in Memory Applications. *2019 IEEE International Electron Devices Meeting (IEDM)*; 2019.

(8) Grossi, A.; Nowak, E.; Zambelli, C.; Pellissier, C.; Bernasconi, S.; Cibrario, G.; Hajjam, K. E.; Crochemore, R.; Nodin, J. F., Fundamental variability limits of filament-based RRAM. *2016 IEEE International Electron Devices Meeting (IEDM)*; 2016.

(9) Lee, B.; Wong, H.-S. P. Fabrication and Characterization of Nanoscale NiO Resistance Change Memory (RRAM) Cells With Confined Conduction Paths. *IEEE Trans. Electron Devices* **2011**, *58*, 3270−3275.

(10) Li, Y.; Fuller, E. J.; Sugar, J. D.; Yoo, S.; Ashby, D. S.; Bennett, C. H.; Horton, R. D.; Bartsch, M. S.; Marinella, M. J.; Lu, W. D.; Talin, A. A. Filament-Free Bulk Resistive Memory Enables Deterministic Analogue Switching. *Adv. Mater.* **2020**, *32*, 2003984.

(11) Mackus, A. J. M.; Merkx, M. J. M.; Kessels, W. M. M. From the Bottom-Up: Toward Area-Selective Atomic Layer Deposition with High Selectivity. *Chem. Mater.* **2019**, *31*, 2−12.

(12) Clark, R.; Tapily, K.; Yu, K.-H.; Hakamata, T.; Consiglio, S.; O'Meara, D.; Wajda, C.; Smith, J.; Leusink, G. Perspective: New Process Technologies Required for Future Devices and Scaling. *APL Mater.* **2018**, *6*, 058203.

(13) Fang, M.; Ho, J. C. Area-Selective Atomic Layer Deposition: Conformal Coating, Subnanometer Thickness Control, and Smart Positioning. *ACS Nano* **2015**, *9*, 8651−8654.
(14) Mackus, A. J. M.; Merkx, M. J. M.; Li, J. Area-selective atomic layer deposition for bottom-up fabrication of nanoelectronics. *Nevac Blad.* **2020**, *58*, 32−34.
(15) Chen, R.; Kim, H.; McIntyre, P. C.; Porter, D. W.; Bent, S. F. Achieving Area-Selective Atomic Layer Deposition on Patterned Substrates by Selective Surface Modification. *Appl. Phys. Lett.* **2005**, *86*, 191910.
(16) Jiang, X.; Bent, S. F. Area-Selective ALD with Soft Lithographic Methods: Using Self-Assembled Monolayers to Direct Film Deposition. *J. Phys. Chem. C* **2009**, *113*, 17613−17625.
(17) Oh, I.; Sandoval, T. E.; Liu, T.-L.; Richey, N. E.; Bent, S. F. Role of Precursor Choice on Area-Selective Atomic Layer Deposition. *Chem. Mater.* **2021**, *33*, 3926−3935.
(18) Seo, S.; Yeo, B. C.; Han, S. S.; Yoon, C. M.; Yang, J. Y.; Yoon, J.; Yoo, C.; Kim, H.-j.; Lee, Y.-b.; Lee, S. J.; Myoung, J.-M.; Lee, H.-B.-R.; Kim, W.-H.; Oh, I.-K.; Kim, H. Reaction Mechanism of AreaSelective Atomic Layer Deposition for Al_2O_3 Nanopatterns. *ACS Appl. Mater. Interfaces* **2017**, *9*, 41607−41617.
(19) De Paula, C.; Richey, N. E.; Zeng, L.; Bent, S. F. Mechanistic Study of Nucleation Enhancement in Atomic Layer Deposition by Pretreatment with Small Organometallic Molecules. *Chem. Mater.* **2020**, *32* (1), 315−325.
(20) Chen, R.; Bent, S. Chemistry for Positive Pattern Transfer Using Area-Selective Atomic Layer Deposition. *Adv. Mater.* **2006**, *18*, 1086−1090.
(21) Singh, J. A.; Thissen, N. F. W.; Kim, W. H.; Johnson, H.; Kessels, W. M. M.; Bol, A. A.; Bent, S. F.; Mackus, A. J. M. Area-Selective Atomic Layer Deposition of Metal Oxides on Noble Metals through Catalytic Oxygen Activation. *Chem. Mater.* **2018**, *30* (3), 663−670.
(22) Baek, I. G.; Kim, D. C.; Lee, M. J.; Kim, H.-J.; Yim, E. K.; Lee, M. S.; Lee, J. E.; Ahn, S. E.; Seo, S.; Lee, J. H.; Park, J. C.; Cha, Y. K.; Park, S. O.; Kim, H. S.; Yoo, I. K.; Chung, U.; Moon, J. T.; Ryu, B. I. Multi-layer cross-point binary oxide resistive memory (OxRRAM) for post-NAND storage application, *IEEE International Electron Devices Meeting, 2005*; IEDM Technical Digest, 2005.
(23) Niu, G.; Calka, P.; Auf der Maur, M.; Santoni, F.; Guha, S.; Fraschke, M.; Hamoumou, P.; Gautier, B.; Perez, E.; Walczyk, C.; Wenger, C.; Di Carlo, A.; Alff, L.; Schroeder, T. Geometric conductive filament confinement by nanotips for resistive switching of HfO_2-RRAM devices with high performance. *Sci. Rep.* **2016**, *6*, 25757.
(24) Misha, S. H.; Tamanna, N.; Woo, J.; Lee, S.; Song, J.; Park, J.; Lim, S.; Park, J.; Hwang, H. Effect of Nitrogen Doping on Variability of TaO_x -RRAM for Low-Power 3-Bit MLC Applications. *ECS Solid State Lett.* **2015**, *4*, P25−P28.
(25) Ielmini, D.; Nardi, F.; Cagli, C. Physical Models of Size-Dependent Nanofilament Formation and Rupture in NiO Resistive Switching Memories. *Nanotechnology* **2011**, *22*, 254022.
(26) Chen, H. P.; Wu, Y. H.; Huang, H. Y.; Tsai, C. H.; Lee, S. K.; Lee, C. C.; Wei, T. H.; Yao, H. C.; Wang, Y. C.; Liao, C. Y.; Chang, H. K.; Lu, C. W.; Shue, W. S.; Cao, M. Fully Self-Aligned Via Integration for Interconnect Scaling Beyond 3nm Node. *IEEE Int. Electron Devices Meet.* **2021**, *21*, 486−489.

https://doi.org/10.1021/acsami.3c05822
ACS Appl. Mater. Interfaces 2023, 15, 43087−43093

Supporting Information

Area-Selective Atomic Layer Deposition for Resistive Random-Access Memory Devices

Il-Kwon Oh[1,2,#,*], Asir Intisar Khan[4,#], Shengjun Qin[4], Yujin Lee[1], H.-S. Philip Wong[4], Eric Pop[4], and Stacey F. Bent[1,*]

[1] *Department of Chemical Engineering, Stanford University, Stanford, CA 94305, USA*

[2] *Department of Electrical and Computer Engineering, Ajou University, Suwon, 16499, South Korea*

[3] *Department of Intelligence Semiconductor Engineering, Ajou University, Suwon, 16499, South Korea*

[4] *Department of Electrical Engineering, Stanford University, Stanford, CA 94305, USA*

[#]*These authors contributed equally to this work.* [*]*E-mail:* ikoh@ajou.ac.kr; sbent@stanford.edu

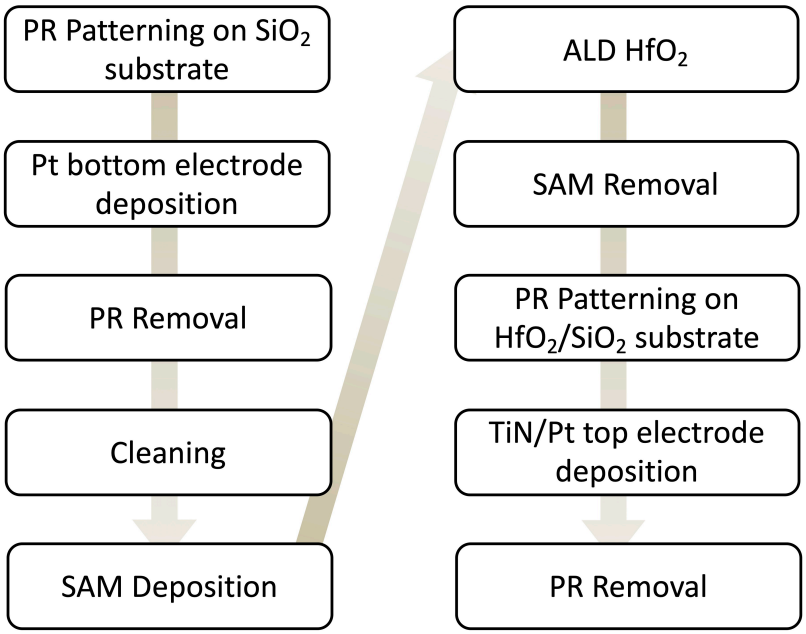


Figure S1. Device fabrication process flow for area-selective atomic layer deposition (ALD) of HfO_2 RRAM. Abbreviation: PR = photoresist, SAM = self-assembled monolayer

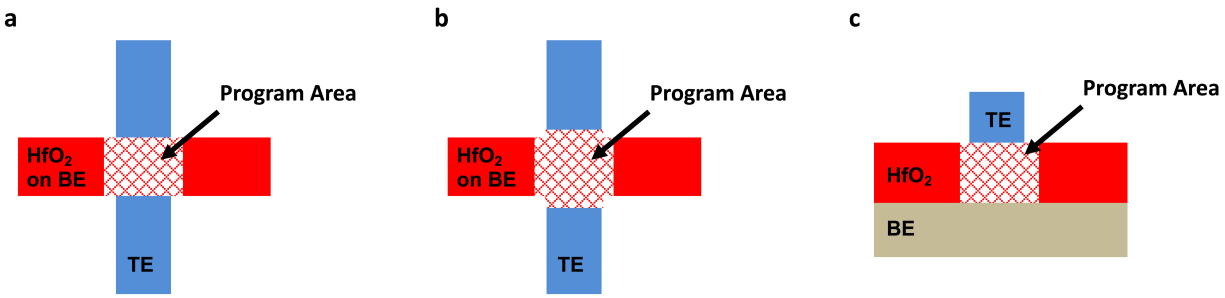


Figure S2. Schematics of fabricated RRAM devices. **a** and **b,** Top-view images for AS-ALD and uniform HfO_2. TE and BE represent top and bottom electrodes, respectively. Program area should be under TE, but for understanding program area easily, the area of TE on program area is removed. **c**, Cross-sectional image of a RRAM device for both AS-ALD and uniform HfO_2.

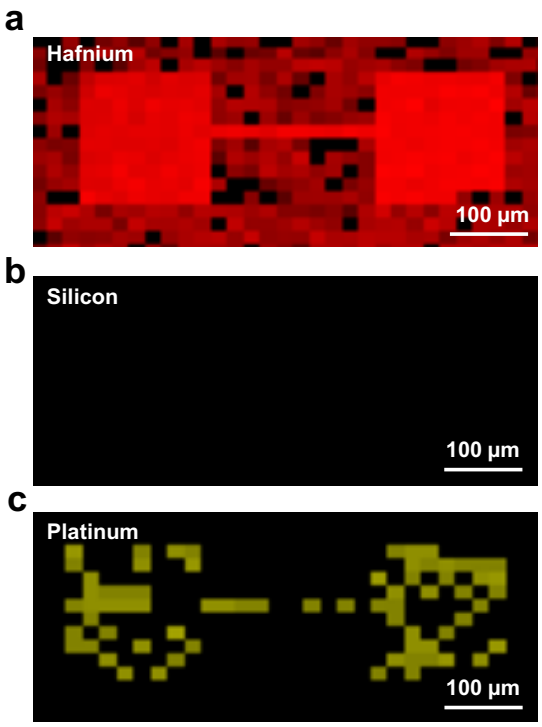


Figure S3. Spatial Auger electron spectroscopy (AES) images of **a**, hafnium, **b**, silicon, and **c,** platinum signals for 50 cycles of ALD of HfO_2 performed without a self-assembled monolayers (SAM) inhibitor on Pt/SiO_2 patterns which are the same as in Figure 2c. Hf signal is observed on both the Pt and SiO_2 regions of the substrate, unlike in the AS-ALD case of Figure 2c for which it is observed only on the Pt.

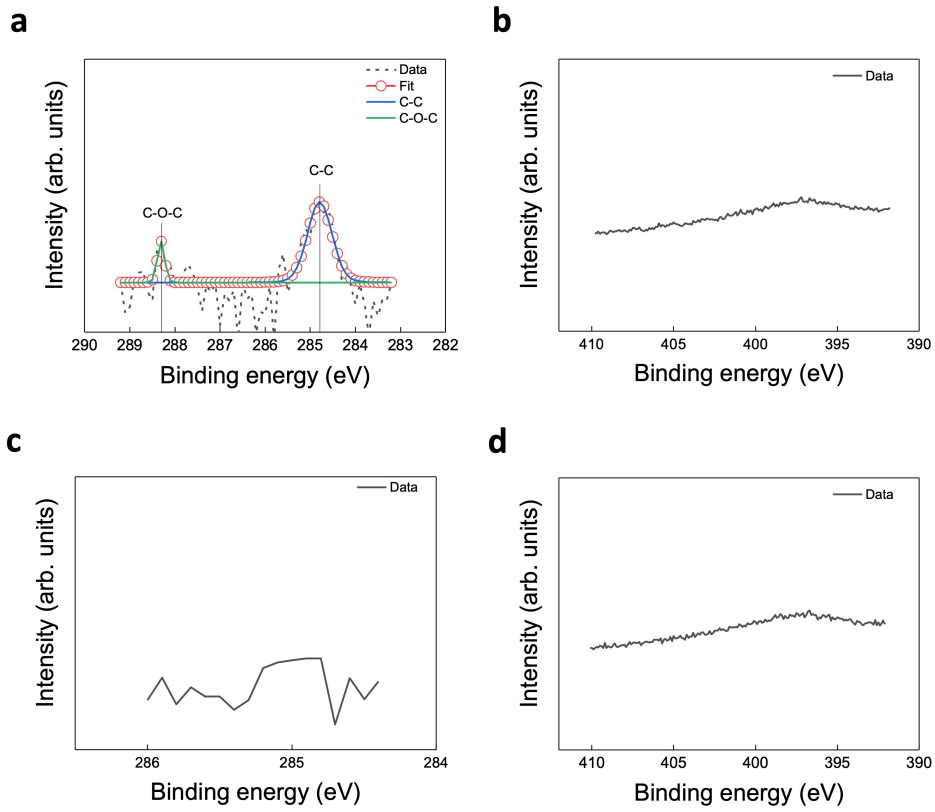


Figure S4. XPS core level spectra: **a,** C 1s and **b**, N 1s for selective HfO_2; **c**, C 1s and **d**, N 1s for uniform HfO_2. Impurity contents in HfO_2 films are compared, to confirm the incorporation of any other impurity when using SAM layers.

Table S1. Atomic concentration of Hf, O, C, and N in selective and uniform HfO_2 films and their stoichiometric ratios measured by XPS.

	Atomic concentration (%)				Stoichiometry ratio	
Elements	Hf	O	C	N	Hf	O
Selective HfO_2	33.1	64.3	0.4	-	1	1.94
Uniform HfO_2	33.4	65.2	-	-	1	1.95

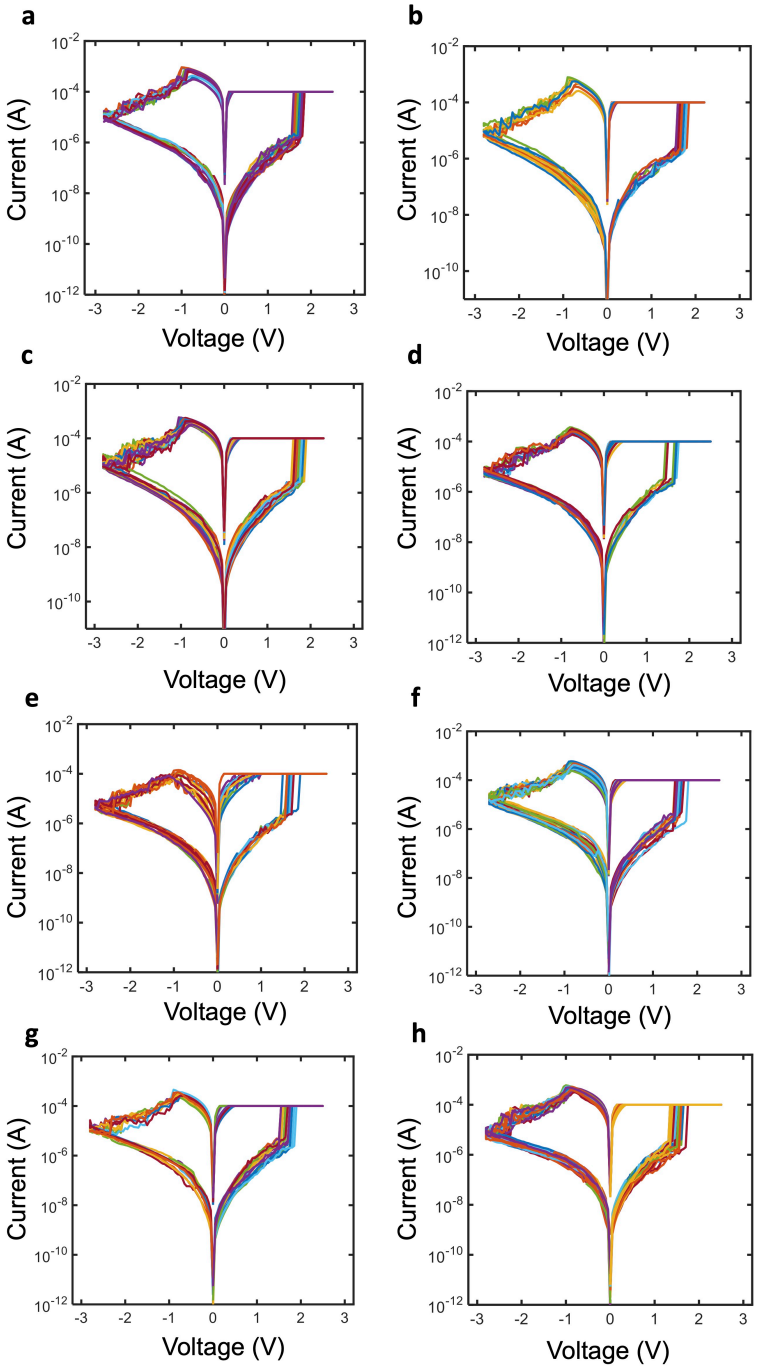


Figure S5. Electrical measurements of additional area-selective ALD RRAM devices. a-h, Current (I) - voltage (V) curves of eight additional RRAM devices fabricated using selective ALD showing low variability in the SET voltage, low and high resistance states (also see **Figure 4** in the main text). All the devices are of 1 x 1 μm^2 in size. Compliance current for the measurements is 100 µA for all the devices.

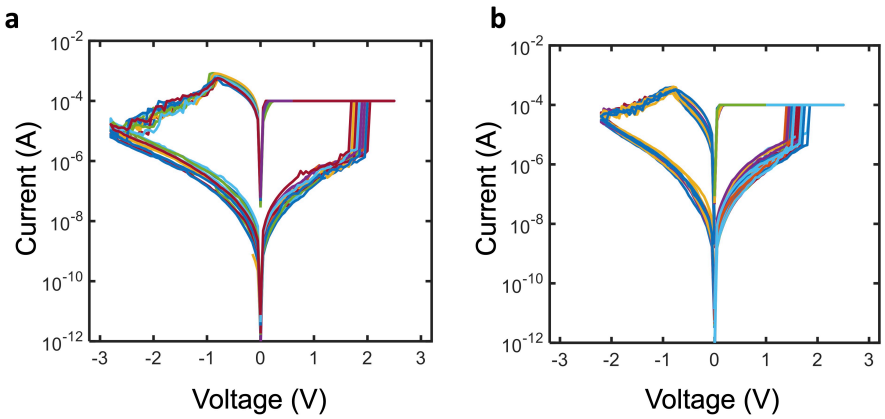


Figure S6. a and **b**, Current (I) - voltage (V) curves of two additional RRAM devices with 2 x 2 μm^2 in size fabricated using selective ALD. Compliance current for the measurements is 100 μA for all the devices.