ARTICLES
https://doi.org/10.1038/s41928-018-0118-9
nature electronics

Electronic synapses made of layered two-dimensional materials

Yuanyuan Shi[1,2], Xianhu Liang[1], Bin Yuan[1], Victoria Chen[2], Haitong Li[2], Fei Hui[1], Zhouchangwan Yu[2], Fang Yuan[2,3], Eric Pop[2], H.-S. Philip Wong[2]* and Mario Lanza[1]*

Neuromorphic computing systems, which use electronic synapses and neurons, could overcome the energy and throughput limitations of today's computing architectures. However, electronic devices that can accurately emulate the short- and long-term plasticity learning rules of biological synapses remain limited. Here, we show that multilayer hexagonal boron nitride (h-BN) can be used as a resistive switching medium to fabricate high-performance electronic synapses. The devices can operate in a volatile or non-volatile regime, enabling the emulation of a range of synaptic-like behaviour, including both short- and long-term plasticity. The behaviour results from a resistive switching mechanism in the h-BN stack, based on the generation of boron vacancies that can be filled by metallic ions from the adjacent electrodes. The power consumption in standby and per transition can reach as low as 0.1 fW and 600 pW, respectively, and with switching times reaching less than 10 ns, demonstrating their potential for use in energy-efficient brain-like computing.

Neuromorphic computing is a brain-inspired information processing model that aims to mimic the efficiency, versatility and resilience of the human brain[1,2]. Synaptic plasticity, the ability of a synapse to alter its connection strength in response to neural activities, is believed to provide the brain with its ability to learn and process information. Long-term plasticity (LTP) enables experience-based learning with a timescale of minutes or longer, and underlies the biological principle for Hebbian learning rules (that is, weight update) for neuromorphic systems[3]. Short-term plasticity (STP) is a dynamic phenomenon where the synaptic strength only changes temporarily on a timescale of milliseconds to minutes, and could enhance the short-term dynamics and responses in neuromorphic systems[4]. Effectively emulating the brain's neuroplasticity in electronic devices, especially synaptic plasticity[5], will be needed if fast and efficient neuromorphic learning machines are expected to be applied to real-time cognitive tasks[6,7].

Hardware implementation of LTP and STP in an integrated neuromorphic system can lead to high energy and area costs when using conventional complementary metal-oxide–semiconductor (CMOS) technologies, as the fundamental synaptic characteristics cannot be efficiently reproduced in a single device[1]. Recent studies have shown that LTP and STP behaviour may be emulated in single devices using resistive switching (RS) electronic synapses[8,9]. The conductance (connection strength) of these two-terminal metal/insulator/metal (MIM) nanoscale devices can be modulated via electrical stimuli[10,11]. By using a wide range of metallic and insulating material combinations, the emulation of LTP and its characteristic features have been achieved, including long-term potentiation, long-term depression, paired-pulse facilitation (PPF), paired-pulse depression (PPD), spike-timing-dependent plasticity (STDP) and spike-rate-dependent plasticity (SRDP)[12–19]. However, even the most advanced MIM-based electronic synapses have difficulty in emulating both STP and LTP in the same device. Primarily, this is due to the stochastic nature of the relaxation process[20,21] within the devices, which can lead to the accumulation of residual charges, and, in turn, a large variability of the relaxation time (τ_{relax}) and device characteristics[8,9,22]. Therefore, previous approaches either used multiple MIM-based devices working in the non-volatile regime[23], a combination of volatile and non-volatile RS devices[22], or bulk materials in a single device that place limitations on device scaling[9]. Currently, there are very few demonstrations of the coexistence of reliable STP and LTP behaviour in single MIM-based RS devices[8,9], which can only be achieved using additional voltage stressing or scanning tunnelling microscope-based modification of the device properties. Despite these advances, controlling the relaxation process and the transition between STP and LTP in electronic synapses remains a major challenge.

Recent studies have revealed that the performance of MIM-based RS devices might be enhanced by introducing layered two-dimensional (2D) materials into their structure[24,25]. Attempts at building electronic synapses using 2D materials have so far used planar configurations, which occupy much more space than vertical MIM cells and cannot be stacked three dimensionally[26–28]. They often suffer from a higher device-to-device variability[25], and, in most cases, the devices are fabricated using mechanical exfoliation[24,26], which is not suitable for building large-area synaptic networks or high-volume-scale manufacturing.

In this Article, we report the fabrication of vertical MIM-based electronic synapses using 2D materials produced by chemical vapour deposition (CVD), a scalable manufacturing-compatible process. By using multilayer hexagonal boron nitride (h-BN) sheets as the RS medium, we have been able to emulate both STP and LTP characteristics in single synaptic devices and observe a very reproducible relaxation process.

Device fabrication and dielectric breakdown

First, we highlight that mechanically exfoliated multilayer h-BN stacks do not show any form of RS, as the dielectric breakdown (BD) is accompanied by irreversible physical damage (such as material removal) due to the absence of native defects

[1]Institute of Functional Nano & Soft Materials, Collaborative Innovation Centre of Suzhou Nanoscience and Technology, Soochow University, Suzhou, China. [2]Department of Electrical Engineering, Stanford University, Stanford, CA, USA. [3]Department of Applied Physics, The Hong Kong Polytechnic University, Hong Kong, China. *e-mail: hspwong@stanford.edu; mlanza@suda.edu.cn

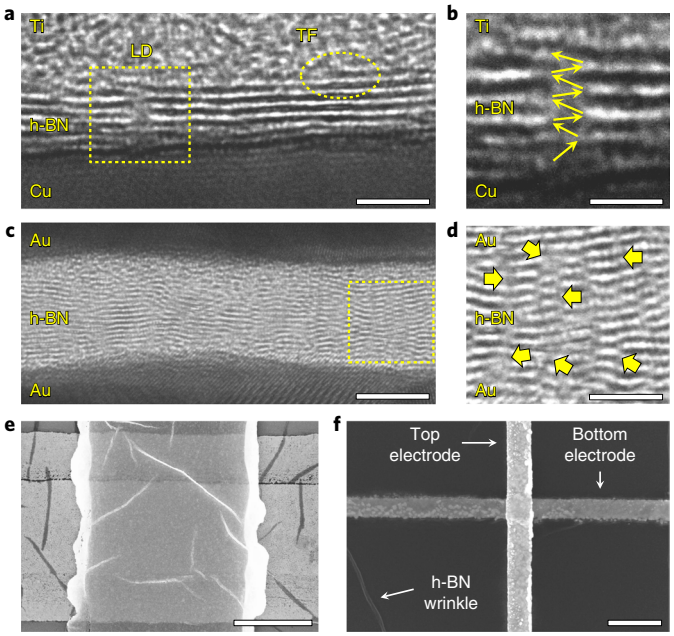

Fig. 1 | Fabrication of metal/h-BN/metal synapses. a,**c**, Cross-sectional TEM images of Au/Ti/5–7-layer h-BN/Cu and Au/15–18-layer h-BN/Au synapses, respectively. **b**,**d**, Zoom-in images of the areas highlighted with dashed squares in **a** and **c**, respectively. LD, lattice disorders; TF, thickness fluctuations. **e**, Top-view scanning electron microscopy (SEM) image of 5 μm × 5 μm Ag/h-BN/Au synapse. **f**, SEM image of a 150 nm × 200 nm Au/Ti/h-BN/Au cross-point synapse. Scale bars: 2 nm (**a**); 1 nm (**b**); 5 nm (**c**); 2 nm (**d**); 2 μm (**e**); 300 nm (**f**).

(Supplementary Fig. 1). However, CVD-grown multilayer h-BN sheets contain a larger amount of native defects that, despite being a nuisance when using the h-BN as a gate dielectric in field-effect transistors or as an anti-scattering substrate, could be useful for RS applications. Following this concept, we synthesized large-area multilayer h-BN sheets by CVD using ammonia borane as the precursor and Cu as the substrate[29–33] (see Methods). The use of a scalable approach (that is, CVD) to synthesize h-BN is an immediate advantage compared with other techniques recently used to prepare 2D materials based RS devices, such as mechanical exfoliation[24,26]. The thickness of the h-BN sheets was varied by tuning the growth parameters (time, temperature, pressure and gas flow), and h-BN sheets with thicknesses of 5–7 layers (Fig. 1a) and 15–18 layers (Fig. 1c) were synthesized. The correct layered structure of the h-BN sheets was corroborated in situ via cross-sectional transmission electron microscopy (TEM). For each sample, more than 80 consecutive TEM images with subnanometre resolution were recorded, covering a total length of ~3 μm (Supplementary Figs. 2 and 3). The TEM images reveal that the h-BN stacks contain native defects consisting of lattice disorders and thickness fluctuations. Interestingly, the lattice disorders appear to propagate out-of-plane, generating defects paths across the layered h-BN stack (Fig. 1b,d). The statistical analysis of all the TEM images revealed that the density of native defects in the h-BN stack increases with the thickness (as happens in HfO_2 and other transition metal oxides[34]), and allowed us to quantify that the percentage of the true layered area can be as high as 90% (for the 5–7-layer-thick sample, see Supplementary Figs. 2 and 3). Using multilayer h-BN as insulator and Au, Ti, Ag and Cu as electrode materials, MIM electronic synapses with different lateral sizes (ranging from 100 μm × 100 μm down to 150 nm × 200 nm) were fabricated (Fig. 1e,f, and Supplementary Figs. 4 and 5). Additional fabrication details can be found in the Methods.

The electronic synapses were first characterized by current versus voltage (I–V) sweeps. Figure 2a shows the first I–V sweep (also called forming process) measured in 15 different 5 μm × 5 μm Au/Ti/15–18-layer h-BN/Au synapses, using a current limitation (CL) of 10 mA. The I–V sweeps show typical tunnelling conduction across the h-BN followed by a sharp current increase, which indicates that the hard BD of the h-BN stack has been triggered[35]. The observation of perfect linear conduction in similar devices without h-BN (Fig. 2a, red line) confirms that the BD event is related to the presence of h-BN. The synapse-to-synapse variability is very low, and comparable to that of RS devices using transition metal oxide (TMO) insulators[36,37] (Supplementary Figs. 6–9). The characteristic sudden current increase observed in the I–V sweeps suggests the formation of one or few conductive nanofilaments (CNF) across the h-BN stack during the BD[38].

To corroborate this hypothesis, the h-BN stacks were stressed using ionic liquid as the top electrode (Supplementary Fig. 10). The advantage of this approach is that after the electrical stress, the ionic liquid can be easily rinsed off and the surface of the h-BN stack is exposed for immediate characterization[39]; this avoids etching a solid top electrode, which can damage the surface of the h-BN. In our study, the h-BN stack was stressed by applying 6 V during 1 min to the ionic liquid, and after that the ionic liquid was rinsed off and the surface of the h-BN was scanned using a conductive atomic force microscope (CAFM). The current maps recorded (Fig. 2c) clearly show the formation of several CNFs across the h-BN stack, the diameters of which range between 5 and 35 nm (Fig. 2d). According to the percolation theory of the BD[40], these CNFs should form at the weakest locations of the dielectric, probably the lattice disorders displayed in Fig. 1b,d, and they may expand laterally depending on the severity of the electrical stress applied[41].

The size and shape of the CNFs in stressed metal/h-BN/metal synapses were analysed in depth from cross-sectional TEM images collected ex situ at different locations. Despite recent set-ups that allow in situ TEM characterization to live monitor the formation of a CNF during the stress[22,24], in this investigation we prefer to carry out an ex situ TEM study because that allows us to work with more realistic devices (the ultra-thin samples and the uncontrollable tip/sample contact force used for in situ TEM studies promote heat confinement and large mechanical stresses[42], which may lead to CNFs with sizes and chemical compositions different than those in real devices). The device selected for this experiment was an Au/Ag/15–18-layer h-BN/Au synapse subjected to an I–V sweep using a CL = 2 mA, and again, more than 80 consecutive TEM images covering a total length of ~3 μm were recorded. In almost all of the images, the h-BN stack showed the correct layered structure with lattice disorders and thickness fluctuations, as those shown in Fig. 1c,d. However, three of them showed the formation of a 10–15 nm wide CNF across the h-BN stack (see Fig. 2e), in good agreement with the CAFM observations (Fig. 2d).

Interestingly, the shape of the I–V sweeps and the BD voltage (V_{BD}) dramatically changes when different top electrode materials are used (Fig. 2b). This is a strong indication that the CNFs are formed by metal ions that penetrate from the electrodes into the h-BN stack under electrical field[43]. This hypothesis was corroborated via electron energy-loss spectroscopy (EELS), which also revealed that metal penetration is always accompanied by the migration of B ions towards the anode (Supplementary Fig. 11). The trapping and de-trapping of charges in the h-BN stack under polarization, which is a characteristic signature of charge exchange in MIM devices, was further confirmed by the observation of random telegraph noise current signals (Supplementary Fig. 12).

Despite the strong parallelism, the switching mechanism in metal/h-BN/metal RS devices is distinct from those observed in redox random access memories (ReRAM, formation of vacancies in the RS medium[44]) and conductive-bridge random access memories

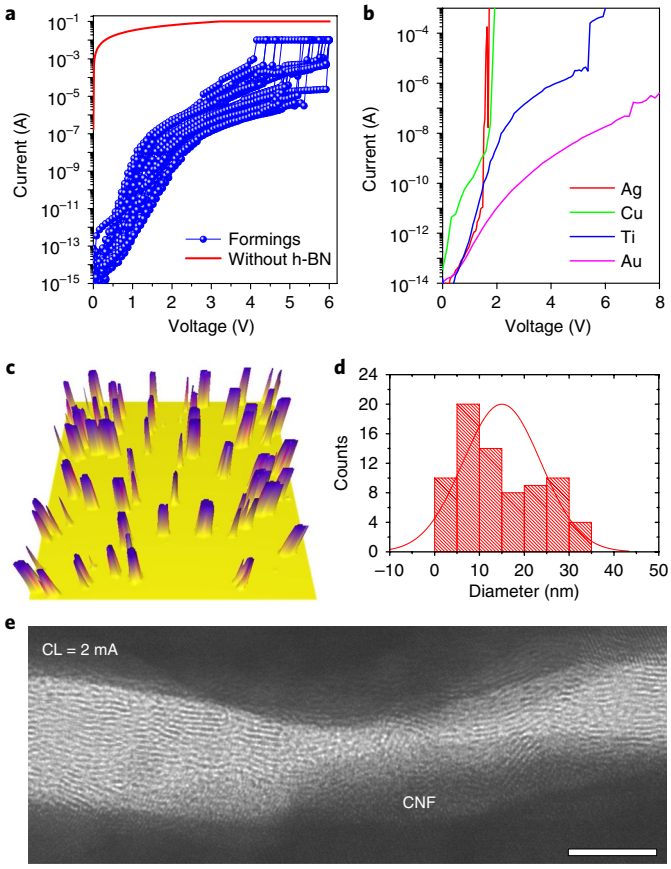

Fig. 2 | Dielectric breakdown in metal/h-BN/metal synapses. a, Typical forming in 15 different 5 μm × 5 μm Au/Ti/15–18-layer h-BN/Au synapses. The red line shows the currents measured in a cross-point structure without h-BN. **b**, Comparison of the forming process in 5 μm × 5 μm metal/h-BN/Au synapses using different top electrode materials. **c**, CAFM current map collected on the surface of the h-BN after applying an electrical stress using ionic liquid (see test structure in Supplementary Fig. 10). The lateral size of the scan is 1 μm × 1 μm; current scale: yellow = 0 nA, blue = 6 nA. **d**, Statistical analysis of the diameter of the CNFs in **c**. The mean value of the normal distribution is 15.00 nm, and the standard deviation is 8.70 nm. **e**, Cross sectional TEM image of one CNF formed in an Au/Ag/15–18-layer h-BN/Au synapse after applying an *I*–*V* sweep using a CL = 2 mA. Scale bar, 4 nm.

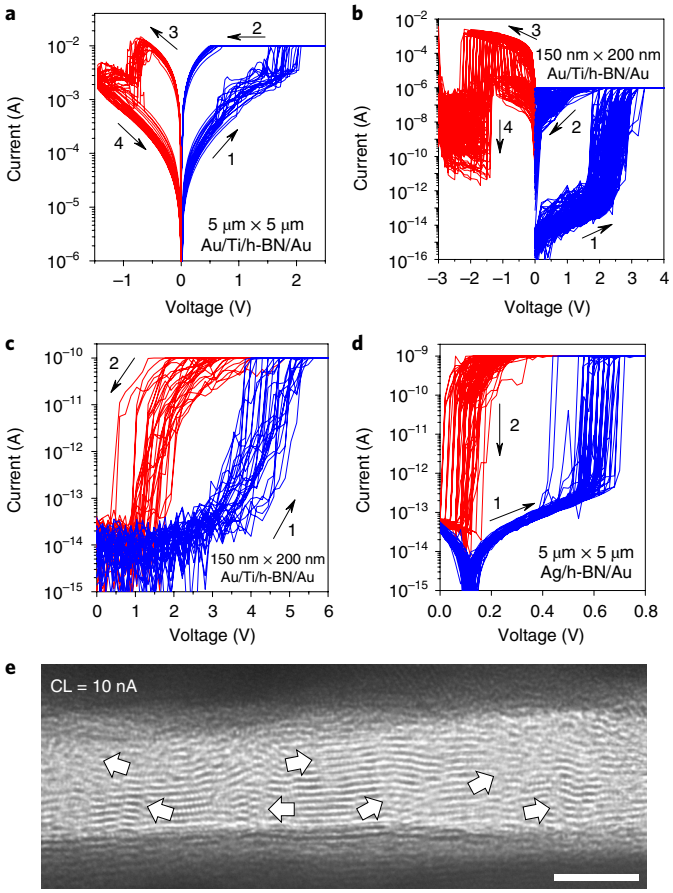

Fig. 3 | Volatile and non-volatile RS in metal/h-BN/metal synapses. a,**b**, Non-volatile bipolar RS for Au/Ti/h-BN/Au synapses with different sizes. **c**, Typical volatile RS observed in the same synapse as in **b**, when a lower (10^{-10} A) CL is used. **d**, Volatile RS in Ag/h-BN/Au synapses. The thickness of the h-BN for all the synapses in **a**–**d** was 15–18 layers. Blue curves represent the set process of the switching and red curves represent the reset process of the switching. The numbers indicate the order in which the *I*–*V* curves were collected. **e**, Representative cross-sectional TEM image of an Au/Ag/15–18-layer h-BN/Au synapse after applying an *I*–*V* sweep using CL = 10 nA (that is, working in the volatile regime). The structure of the h-BN is similar to that in unstressed synapses. At this CL, no large CNFs were detected in more than 80 TEM images, which only show some local defect paths (white arrows). Scale bar, 4 nm.

(CBRAM, metal penetration[45]), as illustrated in Supplementary Fig. 13. In metal/h-BN/metal synapses, the generation of B vacancies leaves behind a N path that, unlike Hf in HfO_2 or Ta in TaO_2, is not conductive enough to drive the large (>100 mA) post-BD currents observed. Therefore, the penetration of metal into h-BN is necessary to form a CNF. However, EELS profiles always indicate the severe migration of intrinsic species (that is, B ions) towards the anode, which does not necessarily happen in metal/TMO/metal RS cells (that is, the switching can be induced only by metal penetration from an active electrode, without O exchange[38]). This novel switching mechanism might be related to the lower activation energy of the B vacancies in the h-BN stack[46], which should be even lower at the lattice disorders[47].

Volatile and non-volatile resistive switching

After the forming process (Fig. 2a), the Au/Ti/15–18-layer h-BN/Au electronic synapses exhibited stable non-volatile RS (Fig. 3a) when *I*–*V* sweeps of opposed polarity were applied (that is, bipolar RS). The current across the synapses could be cyclically switched between a high resistive state (HRS) and a low resistive state (LRS). The observation of non-volatile bipolar RS was highly reproducible for all device areas, and smaller devices exhibited lower HRS currents down to 10 fA at 0.1 V (Fig. 3b). Interestingly, for any device size, the use of lower CLs always resulted in volatile RS (Fig. 3c), in which the synapses recover 100% of their resistivity when the bias is switched off. It should be noted that Au/Ti/HfO_2/Au and Au/Ti/CuO/Au synapses with similar sizes (also fabricated in this study) did not show stable volatile RS (Supplementary Fig. 14)—although some studies have achieved volatile RS in metal/TMO/metal devices[48]. The transition between stable volatile and non-volatile RS in h-BN-based electronic synapses was not abrupt, and a region with unstable RS was observed (Supplementary Figs. 15 and 16). The currents in HRS and LRS, and the set and reset voltages (namely I_{HRS}, I_{LRS}, V_{set} and V_{reset}, respectively) can be tuned using different electrode materials and device sizes. For example, by using Ag top electrodes (that is, Ag/15–18-layer h-BN/Au synapses), V_{set} and V_{reset} can be reduced down to 0.6 V and 0.1 V, respectively, when the synapse is working in volatile mode (Fig. 3d), and the nonlinearity observed in the *I*–*V* sweep is improved.

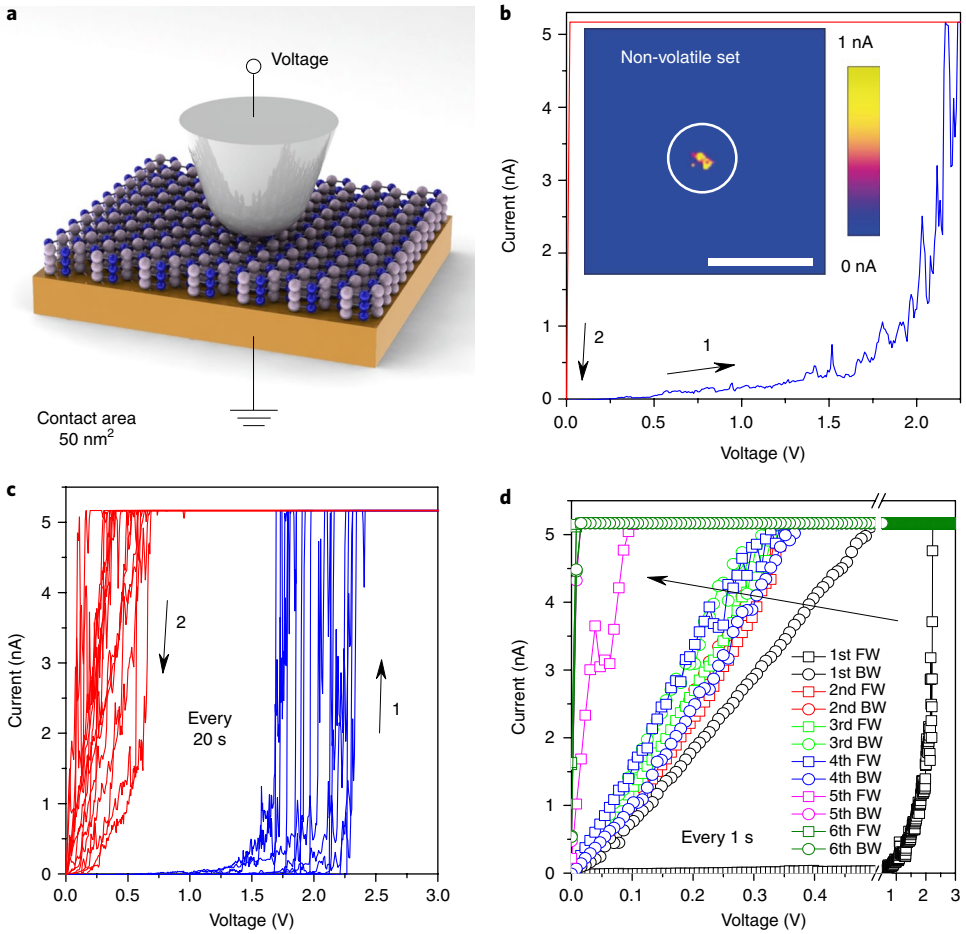

Fig. 4 | In situ observation of volatile and non-volatile RS in h-BN. a, Schematic of the CAFM experiments. The tip/sample junction forms a nanosized Pt/h-BN/Cu synapse. **b**, *I*–*V* sweep from 0 V to 10 V showing non-volatile BD; the part from 2.25 V to 10 V is not shown because it just displays saturated currents at 5.2 nA (see entire plot in Supplementary Fig. 24). The inset is a CAFM current map showing the CNF generated by the *I*–*V* sweep. Scale bar, 80 nm. **c**,**d**, Two sequences of *I*–*V* sweeps from 0 V to 3 V on the same location of the h-BN stack, using time intervals between each cycle of 20 s and 1 s, respectively. Long and short interval times between the *I*–*V* sweeps produce the relaxation/potentiation of the nanosized Pt/h-BN/Cu synapse. The thickness of the h-BN used for this experiment was ~3 layers. In **b** and **c**, blue curves show the forward curves (FW) of the *I*–*V* sweep, and red curves show the backward curves (BW) of the *I*–*V* sweep. The numbers indicate the order in which the *I*–*V* curves were collected in each cycle. The arrow in **d** indicates that the conductivity of the sample increases.

The statistical cross-sectional TEM analysis conducted in a Ag/15–18-layer h-BN/Au synapse working in volatile RS regime (that is, by applying an *I*–*V* sweep with CL = 10 nA) revealed no significant change in the structure of the h-BN (Fig. 3e). The images show some defect paths (Fig. 3e, white arrows) with a shape very similar to that of lattice disorders in the as-grown samples. The corresponding EELS profiles show a composition similar to the unstressed sample, indicating that the stress was not enough high to induce significant atomic rearrangements. Most probably, the charge transport across the h-BN stack in the volatile regime occurs by electron hopping along the defect paths, which could also be considered as atomic-size conductive filaments.

From a power consumption point of view, the Ag/15–18-layer h-BN/Au synapses show I_{HRS} of ~1 fA at a read voltage of 0.1 V (Fig. 3d), which is one of the lowest values in the literature. It is worth noting that the 15–18-layer-thick h-BN stack (5–6 nm) blocked the current out-of-plane similarly (if not better) than ~15-nm-thick HfO_2 films[22]. These numbers imply that, if used as selector device, the power consumption in standby is $P_{standby} = I_{HRS} \times V_{read} = 1$ fA × 0.1 V = 0.1 fW, and the power per set transition is $P_{set} = I_{CL} \times V_{set}$ = 1 nA × 0.6 V = 600 pW. These values might be further improved by tuning the design of the synapses (for example, electrode materials, device size) and also by reducing the CL, as the volatile RS was stable even at lower CLs (that is, CL = 10^{-10} A in Fig. 3c).

The synapses using 5–7-layer-thick h-BN stacks showed non-volatile RS without the need of a forming process (Supplementary Fig. 17), probably due to the ease of some the native lattice disorders to propagate across the entire h-BN stack (Fig. 1a,b). We measured one hundred 5 μm × 5 μm Au/Ti/5–7-layer h-BN/Au synapses and 95 of them showed non-volatile bipolar RS similar to that in Supplementary Fig. 17, with a low synapse-to-synapse variability (see Supplementary Figs. 7–9). This point is especially interesting because variability is one of the main problems of MIM-based RS devices[25,42]. The fact that the metal/h-BN/metal synapses presented here (fabricated in a university lab) show cycle-to-cycle and device-to-device variability comparable to that of meta/TMO/metal RS devices fabricated in an industrial facility[36,37] indicates the great potential of h-BN for this technology.

In situ observation of resistive switching

The volatile and non-volatile RS observations were repeated in situ via CAFM by placing the probe tip in direct contact with the surface of the h-BN, leading to a nano-sized Pt/h-BN/Cu synapse with an effective area of around 7 nm × 7 nm (~50 nm²; ref. [49]). Figure 4a

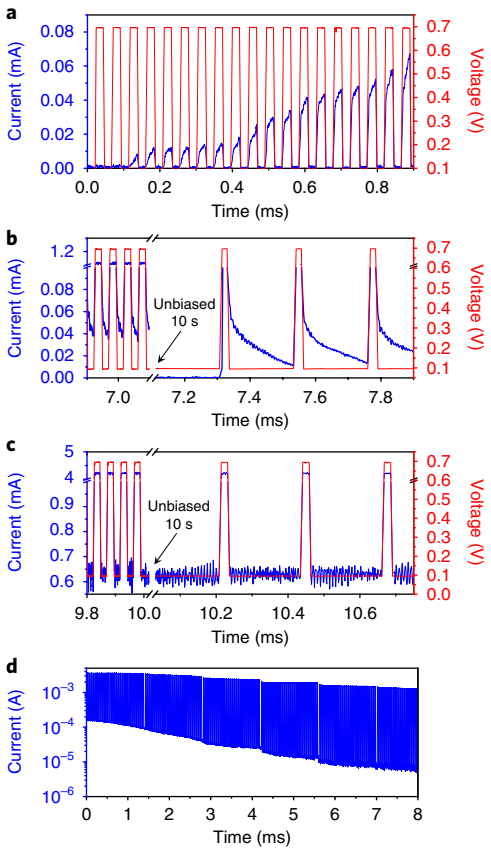

Fig. 5 | Dynamic response of metal/h-BN/metal synapses (type I). a, Sequence of PVS showing synapse potentiation via PPF. **b**, Sequence of PVS showing synapse relaxation with time. The currents during τ_{down} are ~50 µA (volatile regime) and decrease with time; right after 10 s unbiased the currents are ~0.4 µA. **c**, Sequences of PVS showing non-volatile BD. The currents are stable at ~630 µA during τ_{down}, even right after 10 s unbiased. **d**, Current signal measured by applying PVS with V_{down} = −0.1 V and V_{up} = −0.7 V (skipped for clarity), showing a progressive reset transition. This demonstrates the presence of non-volatile RS.

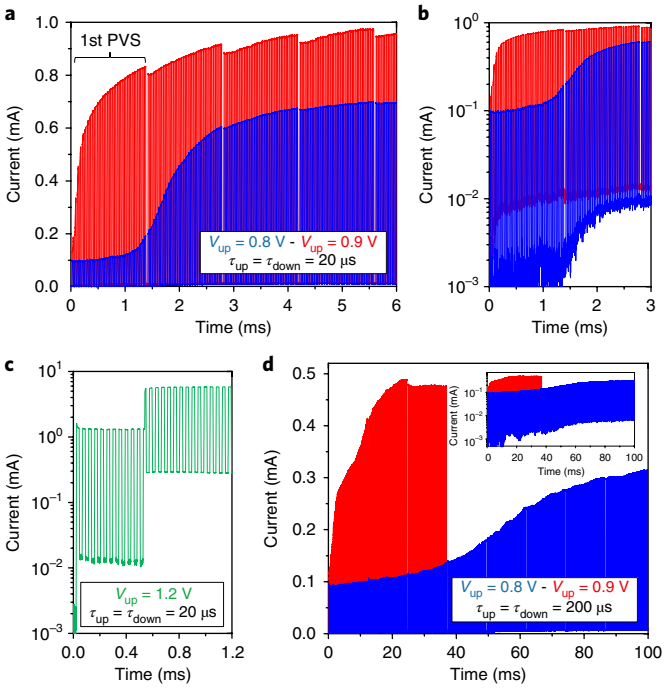

Fig. 6 | Dynamic response of metal/h-BN/metal synapses (type II). a, Two sequences of 4 PVS (with 30 pulses each) collected in a 5 µm × 5 µm 5–7-layer h-BN synapse, showing progressive synapse potentiation with V_{up} = 0.8 V (blue) and V_{up} = 0.9 V (red). V_{down} = 0.1 V and τ_{up} = τ_{down} = 20 µs. **b**, Zoom-in of **a**, with the current in logarithmic scale. **c**, Sequence of PVS with V_{up} = 1.2 V, showing first an abrupt potentiation, and later an additional sudden current increase to the non-volatile RS regime. **d**, Two sequences of PVS showing synapse potentiation with V_{up} = 0.8 V (blue) and V_{up} = 0.9 V (red), using a pulse period τ_{down} = 200 µs, longer than that used in **a**. All plots have been collected on the same device.

shows the schematic of the set-up. When an *I*–*V* sweep from 0 V to 10 V (V_{end}) is applied, the BD event is non-volatile, the conduction during the backward *I*–*V* sweep is perfectly linear, and an ~15-nm-wide CNF can be clearly detected in the subsequent current maps, even after 30 min (Fig. 4b). If V_{end} is reduced (to 3 V), the degree of stress in the h-BN is also lower (similar to using a lower CL in the probe station), and clear volatile RS such as that observed at the device level is detected (Fig. 4c). Subsequent CAFM maps did not detect any CNFs, indicating that the synapse relaxed during the time between the *I*–*V* sweep and the CAFM scan. When the time between the *I*–*V* sweeps was reduced, the current across the synapse increased progressively until it reached the non-volatile regime (Fig. 4d). The conductivity of the synapse, as well as the observation of potentiation or relaxation, depend on the time between the voltage stresses applied and suggests the presence of synaptic plasticity in the metal/h-BN/metal nanojunctions[10].

The self-relaxation of the BD event during volatile RS operation is related to the disruption of the CNF, which is initiated by the de-trapping of some of the metallic ions that were injected into the h-BN during the set event[22,43]. This is a process that depends on time[50], and also on the amount of charges that form the conductive nanofilament (Q_{CNF}), which can be controlled by tuning the CL used during the set *I*–*V* sweep[41]. Therefore, the higher the stress (controlled via CL or V_{end}), the larger the Q_{CNF} and the longer the relaxation time (τ_{relax}).

Statistical analysis of dynamic response

The dynamic response of the h-BN-based synapses was studied in depth by applying sequences of pulsed voltage stresses (PVS) with different amplitudes, durations and intervals (matching the real working conditions), and the currents across them were simultaneously monitored. The electronic synapses selected for this experiment consisted of 50 µm × 50 µm Au/Ti/5–7-layer h-BN/Cu. When stressed via *I*–*V* sweeps, these synapses showed volatile RS for CLs < 100 µA, and non-volatile bipolar RS for CLs > 400 µA (Supplementary Figs. 15 and 16). The synapses were exposed to consecutive trains of PVS, with a pause of 10 s between each train. The voltage up (V_{up}) was 0.7 V, as that is the bias at which the volatile set takes place. The voltage down (V_{down}) was set at 0.1 V in order to monitor the relaxation of the synapse. Time up (τ_{up}) was kept constant at 20 µs, and the time down (τ_{down}) was varied from 20 µs to 200 µs.

Initially, the current across the synapse during τ_{down} (read current) was ~0.4 µA, and it increased progressively (Fig. 5a) until reaching ~50 µA after 150 pulses (Fig. 5b, t = 7.0 ms). This behaviour is suitable for emulating PPF in biological synapses, and further supports the observations in Fig. 4d. It is worth noting that PPF was continuously observed during two orders of magnitude (from ~0.4 µA to ~40 µA, a current range much wider than that shown in previous studies[8,9,22]. When the first train of pulses ended, the synapse relaxed (during the 10 s unbiased), and at the beginning of the second train of pulses, the synapse again showed current levels of ~0.4 µA (Fig. 5b, t = 7.2 ms). This indeed indicates that, even after the application of 150 pulses, the synapse completely relaxed and that no residual charge remained inside the h-BN stack. This hypothesis is

supported by the observation of a longer set time (τ_{set}) during the first pulse after the stop (Fig. 5b, $t=7.3$ ms, $\tau_{SET}=7$ µs), compared with the following pulses (Fig. 5b, $t=7.55$ ms), in which τ_{set} was below the resolution of the set-up (<10 ns; Supplementary Fig. 18).

During τ_{down} the current is not constant but decays fast from 60 µA to 40 µA in 20 µs (Fig. 5b, $t=7.0$ ms). This is consistent with the current levels observed for the volatile RS regime (<100 µA), as shown in Supplementary Fig. 15. To monitor the complete relaxation of the synapses τ_{down} was increased to 200 µs, a time during which the synapse relaxed ~90% of its initial current (Fig. 5b, $t=7.52$ ms). The relaxation process of the Au/Ti/h-BN/Cu synapses was statistically analysed during more than 500 cycles, and minimal variability was detected (Supplementary Fig. 19). The relaxation process of the synapses perfectly matches the exponential power function Kohlrausch law, which is often used by psychologists to characterize memory retention; this is especially interesting because it can be emulated with the discharge of an *RC* circuit, which allows easy simulation at a circuit level using SPICE software (see Supplementary Fig. 20). The time constant of the relaxation process and the minimum currents (before the next pulse) in each cycle were statistically extracted, and are 144.21 ± 12.27 µs and 12.25 ± 1.12 µA, respectively (Supplementary Fig. 20). The fast speed and the low variability of the relaxation process exhibited by the metal/h-BN/metal synapses (Supplementary Fig. 19) are better than those shown in other works (Supplementary Table 1).

If the Au/Ti/5–7-layer h-BN/Cu synapses are further stressed via PVS ($\tau_{up}=\tau_{down}=20$ µs), the currents during both τ_{up} and τ_{down} increase up to ~4 mA and ~0.6 mA, respectively (Fig. 5c). The current during τ_{down} stays constant, indicating that the synapse is working in the non-volatile regime. This conclusion is supported by two facts: (i) the currents during τ_{down} fall within the non-volatile regime, detected via *I*–*V* sweeps (which is >400 µA; Supplementary Fig. 15); and (ii) after the 10 s unbiased, the synapse shows large currents of ~0.6 mA instantaneously (Fig. 5c, $t=10.1$ ms), indicating that the CNFs were not disrupted during the absence of bias. To intentionally disrupt the filaments and relax the synapse, a train of pulses of opposed polarity ($V_{up}=-0.7$ V and $V_{down}=-0.1$ V) was applied, and the conductivity of the synapse decreased smoothly (Fig. 5d), demonstrating the presence of non-volatile bipolar RS. By exposing the synapse to pairs of pre- and post-spikes, we readily observed STDP (Supplementary Fig. 21).

Finally, the dynamic response of 5 µm × 5 µm cross-point Au/Ti/5–7-layer h-BN/Au synapses was analysed by applying sequences of PVS with different pulse voltages and periods. Figure 6a shows two sequences of 4 trains of 30 PVS each, using $\tau_{up}=\tau_{down}=20$ µs, and 2 s pause between each train of pulses. In both cases, $V_{down}=0.1$ V, and V_{up} was selected to be 0.8 V (blue line) and 0.9 V (red line). These PVS were applied in the same synapse, and in both cases the initial resistance was the same (that is, ~100 kΩ at $V=0.1$ V; Fig. 6b). Figure 6a and b both show clear PPF, and the use of a higher V_{up} results in a faster potentiation. The saturation current of the synapse (read during $V_{down}=0.1$ V) reaches 9 µA for $V_{up}=0.8$ V and 13 µA for $V_{up}=0.9$ V (Fig. 6b), and it does not increase anymore even if >1,000 additional pulses are applied. This is opposed to the behaviour observed in Fig. 5, and the reason may be the smaller area of the synapses in Fig. 6, which should contain less weak points and therefore should offer a slower BD process. As Fig. 6b shows, for $V_{up}=0.8$ V the synapse needs 65 pulses to reach 90% of its saturation current, whereas when applying $V_{up}=0.9$ V only 8 pulses are needed. In both cases, if the PVS is stopped, synapse relaxation is observed (see red line in Fig. 6a at $t=1.4$ ms). Therefore, for these current levels the synapse is working in the volatile regime. Indeed, this is consistent with the data collected from *I*–*V* and *I*–*t* curves (Supplementary Fig. 22). If V_{up} is increased to 1.2 V the potentiation of the synapse takes place abruptly in only one pulse (Fig. 6c), and after 12 pulses the current increases again more than one order of magnitude (similarly to the larger synapses shown in Fig. 5). In successive PVS, we observed that the current does not decrease, indicating that the synapse has reached the non-volatile regime. In such case, the conductivity can be restored by applying one *I*–*V* curve with opposed polarity (Supplementary Fig. 23).

Finally, if τ_{up} and τ_{down} are increased to 200 µs, the potentiation of the synapse for $V_{up}=0.8$ V requires a larger amount of pulses (that is, 65 pulses in Fig. 6b versus 300 pulses in Fig. 6d inset). However, when $V_{up}=0.9$ V the number of pulses required for complete potentiation is similar (8 pulses in Fig. 6b and 11 pulses Fig. 6d inset). This observation indicates that V_{up} plays a more important role than τ_{up} and τ_{down} in the dynamics of the synapses. It is worth noting that the number of pulses required to increase the weight of the h-BN based synapses (up to 300) is much larger than that observed in SiO_x- and TMO-based synapses[22], which is beneficial to achieve better potentiation control. As an example, previous works using SiO_x- and TMO-based synapses show erratic conductance transitions, in which the current of one pulse is sometimes smaller than its predecessor[22]; on the contrary, h-BN synapses did not show this erratic behaviour.

Conclusions

We have fabricated electronic synapses using vertical metal/h-BN/metal cells that show both volatile and non-volatile RS simultaneously, which allows emulating several STP and LTP synaptic behaviours, including PPF, PPD, relaxation and STDP. The working regime can be selected by tuning the amplitude, duration and interval of the electrical stimuli. Whereas until now all previous synaptic studies reported slow (0.1–100 s) erratic relaxation process, here we show a fast (~200 µs) and stable relaxation during more than 500 cycles, with a very low variability. The power consumption of the synapses in the volatile regime is 0.1 fW in standby and 600 pW per transition, and we find that the pulse voltage plays a more important role in the potentiation of the synapses than the pulse time/interval. These performances are enabled by a novel switching mechanism that combines characteristics from CBRAM and ReRAM. The volatile and non-volatile nature of the RS has been confirmed at the nanoscale via CAFM, demonstrating excellent potential for scalability. This work represents an important advancement for the development of electronic synapses in terms of performance and, as only scalable processes have been used, the methods described here may be employed to fabricate 2D-materials-based synaptic networks.

Methods

Hexagonal boron nitride growth. Multilayer h-BN stacks were grown by chemical vapour deposition (CVD) on 18-µm-thick Cu foils (JX Nippon Mining & Metals Corporation). Before the growth, the Cu substrate was soaked in acetic acid for 10 h to remove copper oxides, and washed in pure water for 1 min. Several cleaned Cu pieces with sizes ranging between 1 cm × 1 cm and 2 cm × 5 cm were placed at the middle of the quartz tube of the CVD system. Ammonia borane powder (BH_3-NH_3, 97% purity, Sigma-Aldrich) was placed inside an Al_2O_3 boat, and introduced into the sub-chamber of the CVD. The temperature of the furnace was ramped up from room temperature (RT) to 1,000 °C in 40 min, and maintained at 1,000 °C for 80 min. During these first 120 min the atmosphere was 50 s.c.c.m. hydrogen gas flow under a pressure of 645 mTorr. Then the sub-chamber containing the ammonia borane precursor was heated to 100 °C, so that the BH_3-NH_3 could be decomposed to hydrogen, polyiminoborane (BHNH; solid) and borazine ($(HBNH)_3$; gas). The produced borazine gas was carried by 30 s.c.c.m. hydrogen flow from the sub-chamber to the furnace, which was adsorbed on the Cu foil. As a result, multilayer h-BN was formed on the surface of the Cu substrate by borazine thermal decomposition. During the growth, the pressure and the hydrogen flow were maintained at 509 mTorr and 30 s.c.c.m. at 1,000 °C. After the growth finished, the furnace was cooled down to room temperature in 60 min. The thickness and layered structure of the as-grown h-BN was confirmed with cross-sectional TEM (Fig. 1 and Supplementary Figs. 2 and 3).

Fabrication of synapses. Three types of metal/h-BN/metal synapses with different electrode compositions and sizes were fabricated. When referring to metal/h-BN/metal structures, the first metal mentioned is the top electrode (TE) and the second is the bottom electrode (BE), that is, TE/h-BN/BE. The first type of synapse

consisted of Au/Ti/h-BN/Cu cells with sizes of 100 μm × 100 μm and 50 μm × 50 μm (Supplementary Fig. 4), which were fabricated by direct evaporation of Au/Ti electrodes (TE) on the bare surface of the as-grown h-BN/Cu samples. The Ti layer was 20 nm thick (evaporated first, in contact with the h-BN) and the Au layer was 40 nm thick (evaporated second, capping layer). In this process, a laser-patterned shadow mask from Tecan (UK) and an electron-beam evaporator (model PVD75 from Kurt J. Lesker) were used. Supplementary Figure 4 shows a top scanning electron microscope image of the resulting devices. Note that during the fabrication of this type of synapse, we didn't require transfer of the h-BN stack onto a different substrate. The second type consisted of metal/h-BN/Au cross-point devices with sizes ranging from 50 μm × 50 μm down to 5 μm × 5 μm (Fig. 1e and Supplementary Fig. 5). First, bottom electrodes (BE) made of Au(40 nm)/Ti(20 nm) were patterned onto a 300 nm SiO_2/Si wafer via photolithography, metal evaporation and lift-off. The resulting structure was 40 nm Au/20 nm Ti/300 nm SiO_2. The mask aligner used during the photolithography was MJB4 from SUSS MicroTec, and the lift-off process consisted of a bath in acetone for 10–12 h at room temperature. The Ti layer between the Au and SiO_2 was used to enhance the adhesion between these two materials. Then a piece of h-BN was transferred onto the bottom electrodes (see transfer details in the next section). Finally, TEs consisting of Au/Ti, Au/Ag, or Au/Cu were patterned by photolithography. The Au layer was 40 nm thick, while the Ti, Ag or Cu layers were 20 nm thick. One sample using (only) top Au electrodes (60 nm thick) was fabricated as the reference. The third type of synapse consisted of cross-point Au/Ti/h-BN/Au devices very similar to the second type, but with small areas of 150 nm × 200 nm (Fig. 1f). These samples were fabricated by electron-beam lithography (pattern generator (Elphy VII from Raith company) integrated in a Supra 55 scanning electron microscope). Several samples of each type were fabricated on different days, and the data obtained were reproducible. Some devices without h-BN (metal/metal junctions) were fabricated to corroborate that the behaviours observed are produced by the h-BN stack.

Transfer of multilayer h-BN. Liquid poly(methyl methacrylate) (PMMA), made from PMMA powder (Sigma-Aldrich, with average molecular weight ~996,000) dissolved in anisole (40 mg ml^{-1}), was spin-coated on the surface of the multilayer h-BN with a two-step spin-coating process, 500 r.p.m. for 6 s and 3,500 r.p.m. for 30 s, and then baked at 100 °C for 5 min. After that, the Cu foil was etched in $FeCl_3$ (3 mol l^{-1}) for 2–5 h, and the PMMA/h-BN stack was washed in HCl (2 wt%) for 30 s and pure water for 1 h. The PMMA/h-BN stack was picked up with the target substrate (300 nm SiO_2/Si with patterned Au/Ti bottom electrodes), and was dried at 50 °C for 10 min. Finally, the whole sample was immersed in acetone for 10–12 h to remove the PMMA. The presence of h-BN on the target substrate (both SiO_2 and Au/Ti/SiO_2 regions) after the transfer was confirmed by the observation of wrinkles (Fig. 1e,f). Additional discussion about the presence of Cu residues in the h-BN stack can be found in the Supplementary Information.

Device level electrical characterization. Synapses of the first type were characterized using a Cascade probe station (model Summitt 119718) connected to a 4200-SCS Keithley semiconductor analyser at Stanford University. The second and third type of synapses were characterized using a Cascade probe station (model M150) connected to a 4200-SCS Keithley semiconductor analyser at Soochow University. For all *I*–*V* sweeps and pulse mode experiments in Fig. 6 collected in the probe station, the bias was always applied to the top electrode and the bottom was grounded. For the pulse mode experiments (Fig. 5), the bias was applied to the bottom (Cu) electrode and the top (Au/Ti) electrode was grounded. The STDP plot shown in Supplementary Fig. 21 was obtained using a Cascade probe station (SUMMIT 12000B-M) connected to an Agilent semiconductor parameter analyser (B1500A). In total, 186 synapses were characterized in the probe station. The reliability of the data presented is statistically demonstrated along the manuscript and the Supplementary Information, and the variability is reasonably low.

CAFM electrical characterization. Electronic synapses were studied at the nanoscale via CAFM. To do so, the CAFM tip (Pt–Ir-varnished Si tip) was placed on the surface of an as-grown h-BN/Cu sample, and sequences of *I*–*V* sweeps were collected. Before and after this, topographic and current maps were also collected under a constant bias of 2 V, applied to the CAFM tip (top electrode) while keeping the Cu substrate (bottom electrode) grounded. The CAFM used was the Bruker Multimode V working in contact mode using CAFM tips from Nanosensors (model PPP-CONTPt-50). The tip radius was 25 nm, and the force constant 0.02–0.77 N m^{-1}. During the recording of the *I*–*V* curves, the deflection set point was 1 V to ensure good tip/h-BN contact. The current maps after ionic liquid stress in Fig. 2c were collected using Pt-coated silicon tips (Olympus, model AC240TM); their spring constant was 2 N m^{-1} and their tip radius 15 nm.

Ionic liquid-based electrical characterization. The electrical characterization using ionic liquid was carried out by patterning a device structure on the bare surface of the h-BN (Supplementary Fig. 10). To do so, a h-BN/Cu sample was baked at 115 °C for 1.5–2 min to remove water and then spin coated with S1813 photoresist (5,000 r.p.m. for 1 min); after this, the sample was baked again at 115 °C for 2 min. An aperture of 40 μm was patterned via photolithography by exposure for 11 s under a light density of 12 mW cm^{-2}. Then the sample was developed in MF-319 solution for 2.5 min, cleaned with deionized water and dried with N_2 gas. The sample was heated at 180 °C for 2 h to stabilize the photoresist. The second photolithography was then performed with the same procedures as the first to pattern the shape of the top electrode. Then, 40-nm Au contacts were patterned on the photoresist (next to the aperture) via photolithography. Then, the h-BN was contacted to the top metal (on the photoresist) using a drop of ionic liquid (IL, DEME-BF4, $C_8H_{20}NOBF_4$). By using a Cascade probe station (model TRIAX) connected to a Keithley 2636B semiconductor parameter analyser, an electrical field was applied between the top Au electrode and the bottom Cu substrate. More information about this set-up can be found in ref. [39].

Physical characterization. The morphologies of the devices were characterized by optical microscopy (Leica DM4000M) and scanning electron microscopy (Carl Zeiss Supra 55). The surface topography of the materials was characterized by atomic force microscopy (Bruker Multimode V) in tapping mode, using standard silicon tips from Nanoworld (model NCH, $k = 42$ N m^{-1}, $f_0 = 320$ kHz). Cross-sectional TEM (JEOL JEM-2100) was used to confirm the layered structure of the h-BN. The chemical composition of the samples was analysed by an EELS tool integrated in the TEM. Before TEM characterization, thin lamellae were fabricated by a focused ion beam (FEI, HELIOS NANOLAB 450 S).

Data availability. The data that support the plots within this paper and other findings of this study are available from the corresponding authors upon reasonable request.

Received: 5 March 2018; Accepted: 18 July 2018;
Published online: 13 August 2018

References

1. Merolla, P. A. et al. A million spiking-neuron integrated circuit with a scalable communication network and interface. *Science* **345**, 668–673 (2014).
2. Zidan, M. A., Strachan, J. P. & Lu, W. D. The future of electronics based on memristive systems. *Nat. Electron.* **1**, 22–29 (2018).
3. Hyvärinen, A. New approximations of differential entropy for independent component analysis and projection pursuit. In *Advances in Neural Information Processing Systems 10, NIPS Proceedings* 273–279 (Neural Information Processing Systems Foundation, 1997).
4. Zucker, R. S. Short-term synaptic plasticity. *Annu. Rev. Neurosci.* **12**, 13–31 (1989).
5. Abbott, L. F. & Nelson, S. B. Synaptic plasticity: taming the beast. *Nat. Neurosci.* **3**, 1178–1183 (2000).
6. Widrow, B. & Lehr, M. A. 30 years of adaptive neural networks: perceptron, Madaline, and backpropagation. *Proc. IEEE* **78**, 1415–1442 (1990).
7. Li, C. et al. Analogue signal and image processing with large memristor crossbars. *Nat. Electron.* **1**, 52–59 (2018).
8. Chang, T., Jo, S.-H. & Lu, W. Short-term memory to long-term memory transition in a nanoscale memristor. *ACS Nano* **5**, 7669–7676 (2011).
9. Ohno, T. et al. Short-term plasticity and long-term potentiation mimicked in single inorganic synapses. *Nat. Mater.* **10**, 591–595 (2011).
10. Kuzum, D., Yu, S. & Wong, H.-S. P. Synaptic electronics: materials, devices and applications. *Nanotechnology* **24**, 382001 (2013).
11. Wu, H., Yao, P., Gao, B. & Qian, H. Multiplication on the edge. *Nat. Electron.* **1**, 8–9 (2018).
12. Tsuruoka, T., Hasegawa, T., Terabe, K. & Aono, M. Conductance quantization and synaptic behavior in a Ta_2O_5-based atomic switch. *Nanotechnology* **23**, 435705 (2012).
13. Chanthbouala, A. et al. A ferroelectric memristor. *Nat. Mater.* **11**, 860–864 (2012).
14. Li, Y. et al. Activity-dependent synaptic plasticity of a chalcogenide electronic synapse for neuromorphic systems. *Sci. Rep.* **4**, 4906 (2014).
15. Du, C., Ma, W., Chang, T., Sheridan, P. & Lu, W. D. Biorealistic implementation of synaptic functions with oxide memristors through internal ionic dynamics. *Adv. Funct. Mater.* **25**, 4290–4299 (2015).
16. Berdan, R. et al. Emulating short-term synaptic dynamics with memristive devices. *Sci. Rep.* **6**, 18639 (2016).
17. Boyn, S. et al. Learning through ferroelectric domain dynamics in solid-state synapses. *Nat. Commun.* **8**, 14736 (2017).
18. Lashkare, S., Panwar, N., Kumbhare, P., Das, B. & Ganguly, U. PCMO-based RRAM and NPN bipolar selector as synapse for energy efficient STDP. *IEEE Electron Device Lett.* **38**, 1212–1215 (2017).
19. van de Burgt, Y. et al. A non-volatile organic electrochemical device as a low-voltage artificial synapse for neuromorphic computing. *Nat. Mater.* **16**, 414–418 (2017).
20. Cannon, R. C., O'Donnell, C. & Nolan, M. F. Stochastic ion channel gating in dendritic neurons: morphology dependence and probabilistic synaptic activation of dendritic spikes. *PLoS Comput. Biol.* **6**, e1000886 (2010).

21. Yu, S. et al. Stochastic learning in oxide binary synaptic device for neuromorphic computing. *Front. Neurosci.* **7**, 186 (2013).
22. Wang, Z. et al. Memristors with diffusive dynamics as synaptic emulators for neuromorphic computing. *Nat. Mater.* **16**, 101–108 (2017).
23. Werner, T. et al. Experimental demonstration of short and long term synaptic plasticity using OxRAM multi k-bit arrays for reliable detection in highly noisy input data. *2016 IEEE Int. Electron Devices Meet. (IEDM)* https://doi.org/10.1109/IEDM.2016.7838433 (2016).
24. Wang, M. et al. Robust memristors based on layered two-dimensional materials. *Nat. Electron.* **1**, 130–136 (2018).
25. Hui, F. et al. Graphene and related materials for resistive random access memories. *Adv. Electron. Mater.* **3**, 1600195 (2017).
26. Tian, H. et al. Anisotropic black phosphorus synaptic device for neuromorphic applications. *Adv. Mater.* **28**, 4991–4997 (2016).
27. Tian, H. et al. Graphene dynamic synapse with modulatable plasticity. *Nano Lett.* **15**, 8013–8019 (2015).
28. Tian, H. et al. A novel artificial synapse with dual modes using bilayer graphene as the bottom electrode. *Nanoscale* **9**, 9275–9283 (2017).
29. Hui, F. et al. On the use of two dimensional hexagonal boron nitride as dielectric. *Microelec. Eng.* **163**, 119–133 (2016).
30. Kim, K. K. et al. Synthesis and characterization of hexagonal boron nitride film as a dielectric layer for graphene devices. *ACS Nano* **6**, 8583–8590 (2012).
31. Song, L. et al. Large scale growth and characterization of atomic hexagonal boron nitride layers. *Nano Lett.* **10**, 3209–3215 (2010).
32. Lee, K. H. et al. Large-scale synthesis of high-quality hexagonal boron nitride nanosheets for large-area graphene electronics. *Nano Lett.* **12**, 714–718 (2012).
33. Shi, Y. et al. Coexistence of volatile and non-volatile resistive switching in 2D h-BN based electronic synapses. *2017 IEEE Int. Electron Devices Meet. (IEDM)* https://doi.org/10.1109/IEDM.2017.8268333 (2017).
34. Lanza, M. et al. Influence of the manufacturing process on the electrical properties of thin (<4nm) hafnium based high-k stacks observed with CAFM. *Microelectron. Reliab.* **47**, 1424–1428 (2007).
35. Weinberg, Z. A. & Nguyen, T. N. The relation between positive charge and breakdown in metal-oxide-silicon structures. *J. Appl. Phys.* **61**, 1947–1956 (1987).
36. Chen, Y. Y. et al. Tailoring switching and endurance/retention reliability characteristics of HfO_2/Hf RRAM with Ti, Al, Si dopants. *2014 Symp. VLSI Tech.* https://doi.org/10.1109/VLSIT.2014.6894403 (2014).
37. Belmonte, A. et al. A thermally stable and high-performance 90-nm Al_2O_3/Cu-based 1T1R CBRAM cell. *IEEE Trans. Electron Dev.* **60**, 3690–3695 (2013).
38. Xiao, N. et al. Resistive random access memory cells with a bilayer TiO_2/SiO_x insulating stack for simultaneous filamentary and distributed resistive switching. *Adv. Funct. Mater.* **27**, 1700384 (2017).
39. Tang, K. et al. Distinguishing oxygen vacancy electromigration and conductive filament formation in TiO_2 resistance switching using liquid electrolyte contacts. *Nano Lett.* **17**, 4390–4399 (2017).
40. Suñé, J. et al. On the breakdown statistics of very thin SiO_2 films. *Thin Solid Films* **185**, 347–362 (1990).
41. Uppal, H. J. Breakdown and degradation of ultrathin Hf-based $(HfO_2)_x(SiO_2)_{1-x}$ gate oxide films. *J. Vac. Sci. Technol. B* **27**, 443–447 (2009).
42. Lanza, M. et al. Recommended methods to study resistive switching devices. *Adv. Electron. Mater.* (in the press).
43. Yang, Y. et al. Electrochemical dynamics of nanoscale metallic inclusions in dielectrics. *Nat. Commun.* **5**, 4232 (2014).
44. Waser, R., Dittmann, R., Staikov, G. & Szot, K. Redox-based resistive switching memories—nanoionic mechanisms, prospects, and challenges. *Adv. Mater.* **21**, 2632–2663 (2009).
45. Valov, I., Waser, R., Jameson, J. R. & Kozicki, M. N. Electrochemical metallization memories—fundamentals, applications, prospects. *Nanotechnology* **22**, 254003 (2011).
46. Zobelli, A., Ewels, C. P., Gloter, A. & Seifert, G. Vacancy migration in hexagonal boron nitride. *Phys. Rev. B* **75**, 094104 (2007).
47. Pan, F., Gao, S., Chen, C., Song, C. & Zeng, F. Recent progress in resistive random access memories: materials, switching mechanisms, and performance. *Mater. Sci. Eng. R* **83**, 1–59 (2014).
48. Cortese, S., Trapatseli, M., Khiat, A., & Prodromakis, T. A TiO2-based volatile threshold switching selector device with 107 non linearity and sub 100 pA off current. *2016 Int. Symp. VLSI Tech. Syst. Appl.* https://doi.org/10.1109/VLSI-TSA.2016.7480484 (2016).
49. Frammelsberger, W., Benstetter, G., Kiely, J. & Stamp, R. C-AFM-based thickness determination of thin and ultra-thin SiO_2 films by use of different conductive-coated probe tips. *Appl. Surf. Sci.* **253**, 3615–3626 (2007).
50. Jonscher, A. K. Dielectric relaxation in solids. *J. Phys. D* **32**, R57–R70 (1999).

Acknowledgements

This work was supported by the member companies of the Non-Volatile Memory Technology Research Initiative (NMTRI) at Stanford University, the National Science Foundation EFRI 2-DARE EFRI: Energy-Efficient Electronics with Atomic Layers (E3AL) (award no. 1542883), the National Science Foundation of China (grants 61502326, 41550110223, 11661131002), the Jiangsu Government (grant BK20150343), and the Ministry of Finance of China (grant SX21400213). P. C. McIntyre and K. Tang (Stanford University) are acknowledged for support with ionic liquid experiments. Q. Liu and X. Zhang (IMECAS) are acknowledged for support with the STDP experiments. M. A. Villena and X. Jing are acknowledged for support with the SPICE simulation and mechanical exfoliation of h-BN, respectively.

Author contributions

M.L., Y.S., E.P. and H.-S.P.W. designed the experiments. Y.S., V.C. and F.H. grew the h-BN stacks. Y.S. and X.L. fabricated the electronic synapses using photolithography, and B.Y. fabricated the electronic synapses using electron-beam lithography. Y.S., X.L., B.Y, Z.Y. and F.Y. characterized the devices. Y.S., H.L., M.L. and H.-S.P.W. wrote the manuscript. All authors discussed the data and results.

Competing interests

The authors declare no competing interests.

Additional information

Supplementary information is available for this paper at https://doi.org/10.1038/s41928-018-0118-9.

Reprints and permissions information is available at www.nature.com/reprints.

Correspondence and requests for materials should be addressed to H.-S.P.W. or M.L.

Publisher's note: Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.