

2D Materials



LETTER

Intrinsic electrical transport and performance projections of synthetic monolayer MoS₂ devices

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E-mail: epop@stanford.edu**Keywords:** MoS₂, monolayer, transfer length method, effective mobility, current densitySupplementary material for this article is available [online](#)

Abstract

We demonstrate monolayer (1L) MoS₂ grown by chemical vapor deposition (CVD) with transport properties comparable to those of the best exfoliated 1L devices over a wide range of carrier densities (up to $\sim 10^{13} \text{ cm}^{-2}$) and temperatures (80–500 K). Transfer length measurements decouple the intrinsic material mobility from the contact resistance, at practical carrier densities ($> 10^{12} \text{ cm}^{-2}$). We demonstrate the highest current density reported to date ($\sim 270 \mu\text{A } \mu\text{m}^{-1}$ or 44 MA cm^{-2}) at 300 K for an 80 nm long device from CVD-grown 1L MoS₂. Using simulations, we discuss what improvements of 1L MoS₂ are still required to meet technology roadmap requirements for low power and high performance applications. Such results are an important step towards large-area electronics based on 1L semiconductors.

1. Introduction

Monolayer (1L) two-dimensional (2D) semiconductors such as MoS₂ have garnered attention for highly scaled optoelectronics and flexible electronics due to their sub-nm thickness, direct band gap, and lack of dangling bonds [1, 2]. For practical applications, such films must be grown over large areas and must demonstrate good electrical properties. Until recently [3–9], however, the highest reported mobility of 1L MoS₂ field effect transistors (FETs) grown by chemical vapor deposition (CVD) had been below $20 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ on isolated single crystals [10–24]. In addition, little systematic work has been done to understand metallic contacts to CVD-grown 1L films [25], which ultimately limit device performance with scaling.

Here we present the first rigorous transfer length method (TLM) study of as-grown 1L CVD MoS₂ devices as a function of temperature, to systematically separate contributions to total device resistance (R_{TOT}) from contacts and the channel. Building on previous work to improve contact resistance (R_c) [26] we obtain $R_c \approx 6.5 \text{ k}\Omega \mu\text{m}$ at room temperature and moderate carrier densities. We also extract the effective electron mobility (μ_{eff}) from sheet resistance

measurements to be $\sim 20 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, comparable to unencapsulated exfoliated 1L devices on SiO₂. Fitting with our compact model [27, 28] yields similar values for R_c and μ_{eff} and allows us to simulate aggressively scaled device channel lengths (L) while maintaining the key material properties. With an equivalent oxide thickness (EOT) and R_c values dictated by future International Technology Roadmap for Semiconductors (ITRS) requirements, the simulations predict that for both the high performance (HP) and low power (LP) specifications, the maximum achievable on-state current (I_{ON}) is more strongly dependent on the saturation velocity, v_{sat} , than on mobility.

2. Methods

We synthesize continuous 1L MoS₂ from solid S and MoO₃ precursors with the aid of perylene-3,4,9,10 tetracarboxylic acid tetrapotassium salt (PTAS) [10, 11, 29, 30] on SiO₂ on Si (p⁺⁺) substrates, which also serve as back-gates for field-effect devices. Elevated temperature (850 °C) and atmospheric pressure are utilized to encourage lateral epitaxial growth (figures S1 and S2), and the CVD conditions can be tailored to produce either a continuous 1L film or

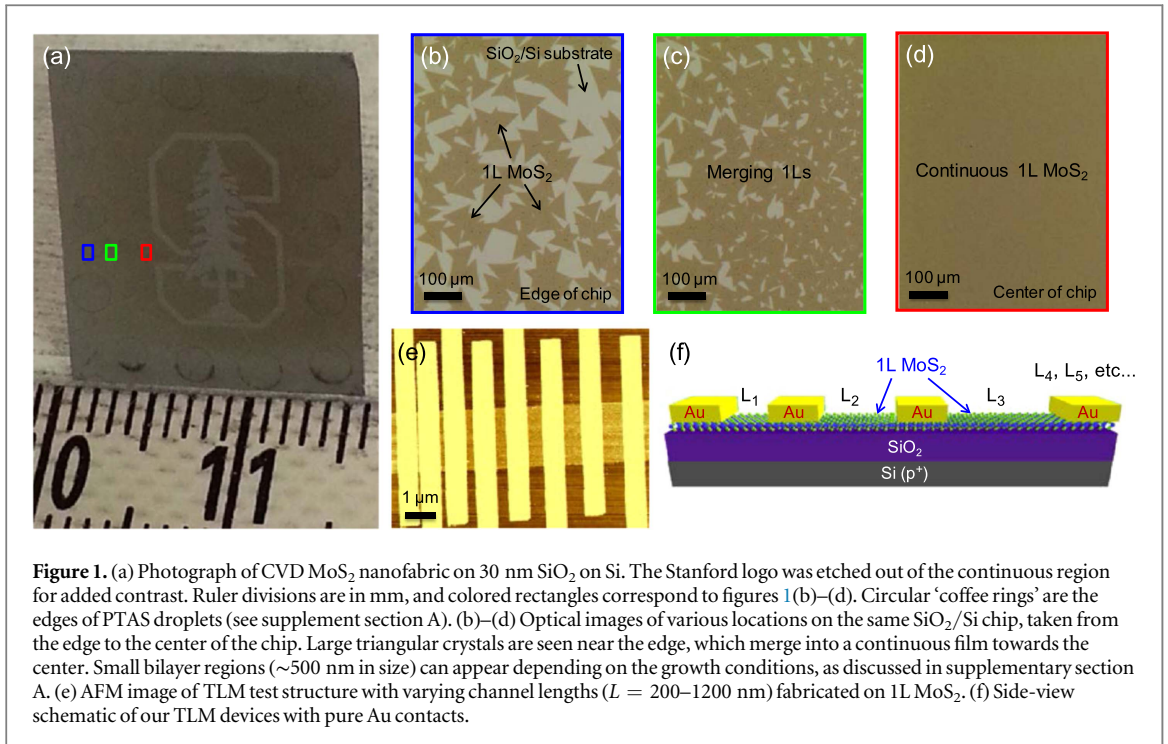


Figure 1. (a) Photograph of CVD MoS₂ nanofabric on 30 nm SiO₂ on Si. The Stanford logo was etched out of the continuous region for added contrast. Ruler divisions are in mm, and colored rectangles correspond to figures 1(b)–(d). Circular ‘coffee rings’ are the edges of PTAS droplets (see supplement section A). (b)–(d) Optical images of various locations on the same SiO₂/Si chip, taken from the edge to the center of the chip. Large triangular crystals are seen near the edge, which merge into a continuous film towards the center. Small bilayer regions (~500 nm in size) can appear depending on the growth conditions, as discussed in supplementary section A. (e) AFM image of TLM test structure with varying channel lengths ($L = 200\text{--}1200$ nm) fabricated on 1L MoS₂. (f) Side-view schematic of our TLM devices with pure Au contacts.

single-crystal domains up to $10^5 \mu\text{m}^2$ (triangular crystals with edges exceeding $300 \mu\text{m}$, see figures 1(a)–(d) and supplementary figure S3). Key advances in this work include a combination of PTAS seeding around the chip perimeter, higher synthesis temperatures, and improved electrical contacts with pure Au, which lead to the improved device results shown here. Previous studies that implemented PTAS for CVD growth did not have high-quality electrical data due to (relatively) poor electrical contacts or small grain sizes. Conversely, previous studies that made contact improvements focused on exfoliated multi-layer MoS₂, not on CVD-grown 1L. Additional discussion about various growth conditions and their optimization is provided in the supplement.

We define rectangular channel regions by XeF₂ etching, and TLM [31] structures with varying channel lengths ($L = 80$ nm to $1.2 \mu\text{m}$) by electron beam (e-beam) lithography, exclusively on 1L regions, as shown in figures 1(e) and (f). Pure Au contacts deposited by e-beam evaporation under high vacuum ($\sim 5 \times 10^{-8}$ Torr) are employed without any adhesion layer to achieve a clean contact interface and reduce contact resistance [26]. All electrical measurements were carried out in a vacuum probe station ($\sim 10^{-5}$ Torr) following a vacuum anneal *in situ* at 200°C for 1 h.

Atomic force microscopy (AFM), Raman spectroscopy, and photoluminescence are utilized post-fabrication to confirm that the MoS₂ devices are indeed 1L [32–34], and that their vibrational and excitonic properties have been preserved. Figure 2(a) illustrates an AFM step-height profile of ~ 1 nm, which is consistent with the 1L MoS₂ thickness plus a van der Waals gap. Figure 2(b) depicts the in-plane and out-

of-plane Raman modes, which are sometimes incorrectly labeled E_{2g} and A_{1g} in the literature; this notation is only strictly correct for bulk and even-number-layer samples, which belong to the D_{6h} and D_{3d} point groups, respectively. Odd-numbered few-layer MoS₂ samples (including 1L) belong to the D_{3h} point group. Thus, these Raman features are denoted as E' and A_1' [35–37] at 383.4 and 403.7 cm^{-1} , with a peak separation $\Delta f \sim 20 \text{ cm}^{-1}$ [4, 5, 9] typical for as-grown MoS₂ 1L with slight intrinsic tensile strain. Lastly, the A and B exciton peaks, estimated to be separated by a valence band splitting of ~ 150 meV at the K point [34, 38] are clearly exhibited with peaks at 1.79 and 1.93 eV.

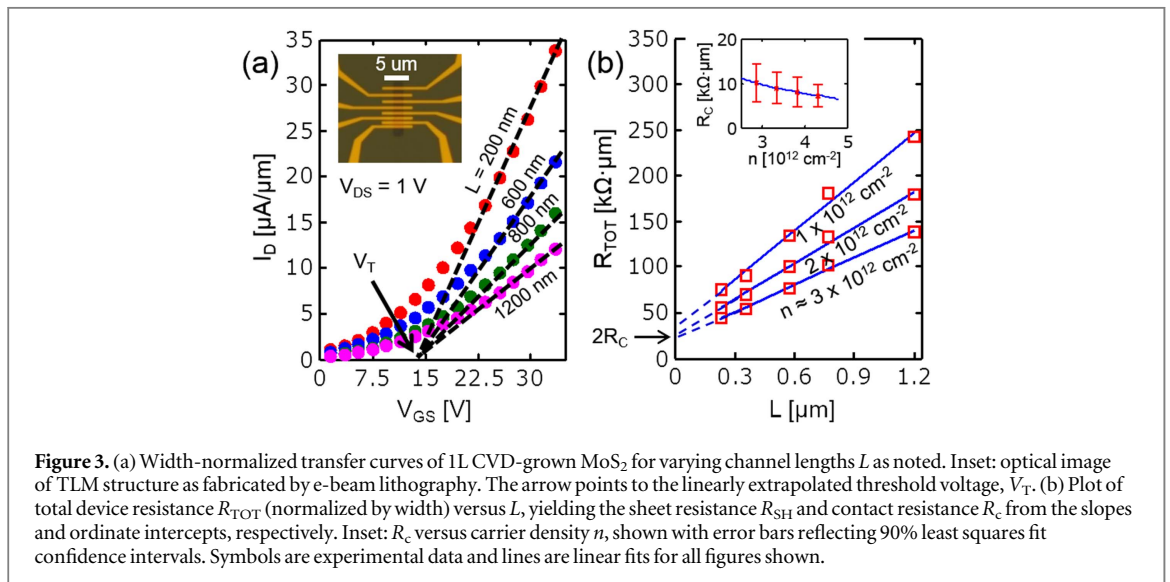
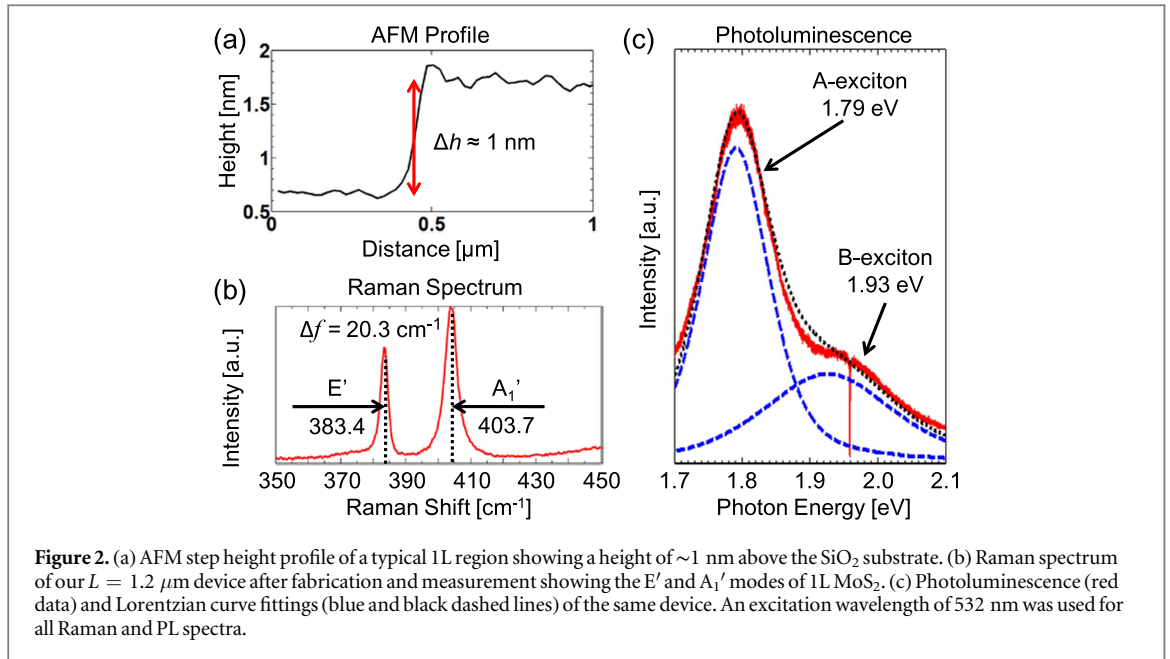
3. Experimental results and discussion

Typical current vs. gate voltage measurements for these devices with varying channel lengths are shown in figure 3(a) at a drain bias $V_{DS} = 1$ V. The carrier density (n) is estimated by assuming a simple linear charge dependence on the gate voltage overdrive

$$n \approx \frac{C_{\text{ox}}}{q} (V_{GS} - V_T), \quad (1)$$

where $C_{\text{ox}} \approx 38 \text{ nF cm}^{-2}$ is the capacitance per unit area of $t_{\text{ox}} = 90$ nm SiO₂. V_{GS} is the gate-source voltage and V_T is the threshold voltage obtained by the linear extrapolation method for each channel [31] as shown in figure 3(a) (dashed lines fit to the curve at maximum transconductance). Supplementary figure S4 displays log-scale and forward-backward I_D - V_{GS} sweeps of the same devices, demonstrating $I_{\text{ON}}/I_{\text{OFF}}$ of at least 10^4 and minimal hysteresis.

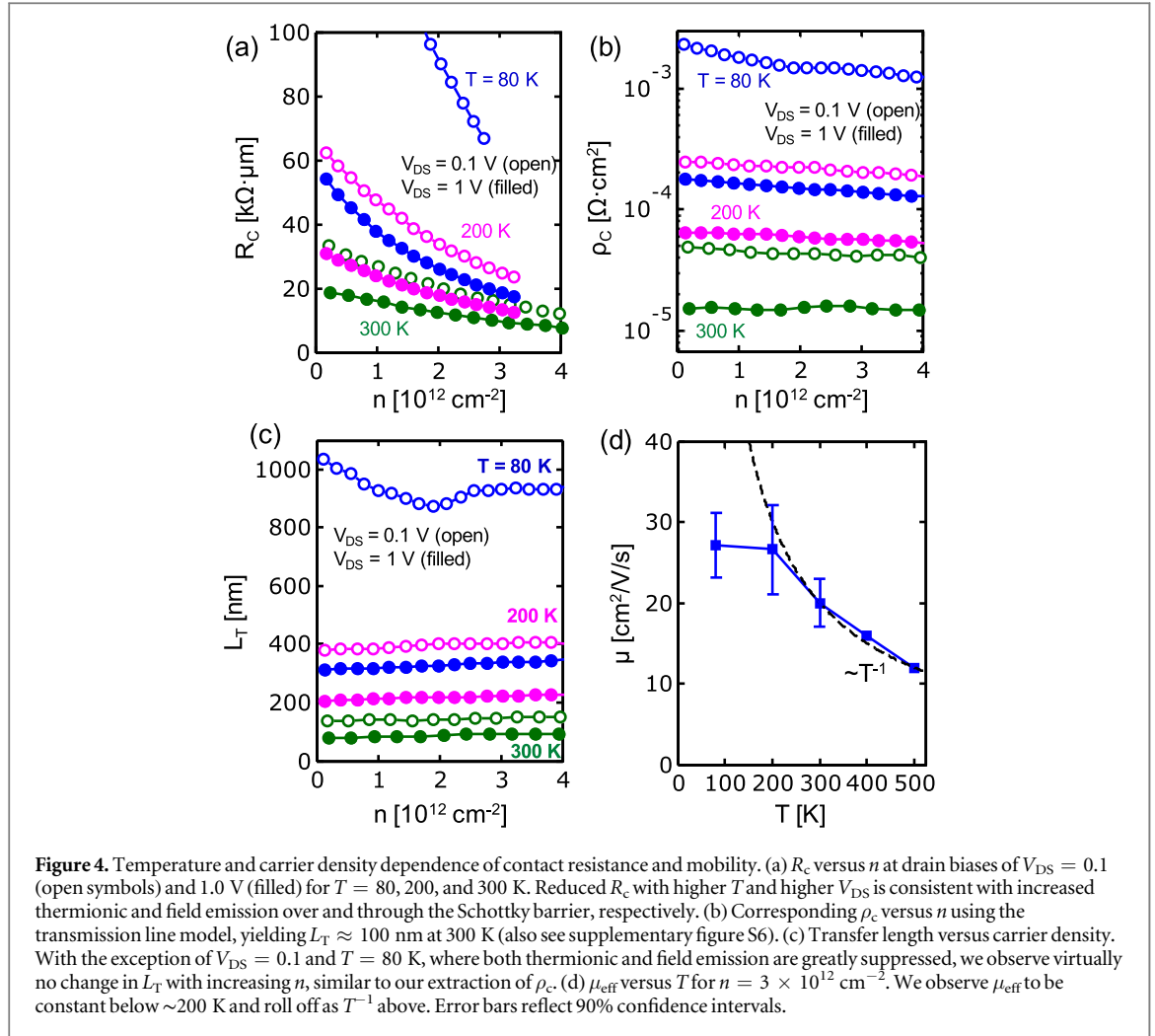
Figure 3(b) demonstrates good least-squares fitting to R_{TOT} versus L for various calculated values of n ,



suggesting uniform material and contacts for our devices. The slopes of these lines correspond to the sheet resistance R_{SH} ($\text{k}\Omega/\square$), whereas the ordinate intercept yields twice the width-normalized contact resistance, $2R_c$ ($\text{k}\Omega \mu\text{m}$); these quantities are extracted for multiple values of n . Resistance and mobility values are then carefully obtained for the same value of n (i.e. the same gate overdrive, $V_{\text{GS}} - V_T$) rather than the same V_{GS} . We note that it is important to perform such TLM extractions from a wide range of channel lengths (including some well below $1 \mu\text{m}$) in order to minimize the R_c error [26].

In figure 4(a), we observe that R_c varies with n as the back gate modulates the Fermi level under the contacts as well as in the channel. We extract $R_c = 6.5 \pm 1.5 \text{ k}\Omega \mu\text{m}$ at 300 K for $n \approx 4 \times 10^{12} \text{ cm}^{-2}$, with the uncertainty reflecting 90% confidence intervals from a

least squares fit of the TLM curve. Although lower R_c has been achieved in multilayer exfoliated MoS_2 FETs [26, 39], this value for 1L CVD MoS_2 could potentially be reduced further with the aid of chemical doping techniques [39–41] or phase engineering [25, 42]. Moreover, fitting with our compact model [27, 28] and extrapolating to a higher $n = 10^{13} \text{ cm}^{-2}$, R_c could drop to $5.5 \text{ k}\Omega \mu\text{m}$, without any kind of molecular doping or threshold shifting, for pure Au contacts. R_c also decreases with increasing temperature (T), consistent with increased thermionic emission over the Schottky barrier at the contacts. Lastly, we note that although our devices exhibit a linear $I_D - V_{\text{DS}}$ relationship for low drain biases (see supplementary figure S5), this does not justify use of the word ‘Ohmic’ to characterize our contacts from a band structure perspective [43]. Linear $I_D - V_{\text{DS}}$ curves can still be



obtained at low bias across a Schottky-barrier FET as a result of carriers tunneling through the barrier, resulting in non-negligible contact resistance [44–46].

Using the transmission line model [31, 47], we estimate the specific contact resistivity (ρ_c) as shown in figure 4(b) from

$$R_c = \frac{\rho_c}{L_T} \coth\left(\frac{L_c}{L_T}\right) \approx \sqrt{\rho_c R_{\text{SH}}}, \quad (2)$$

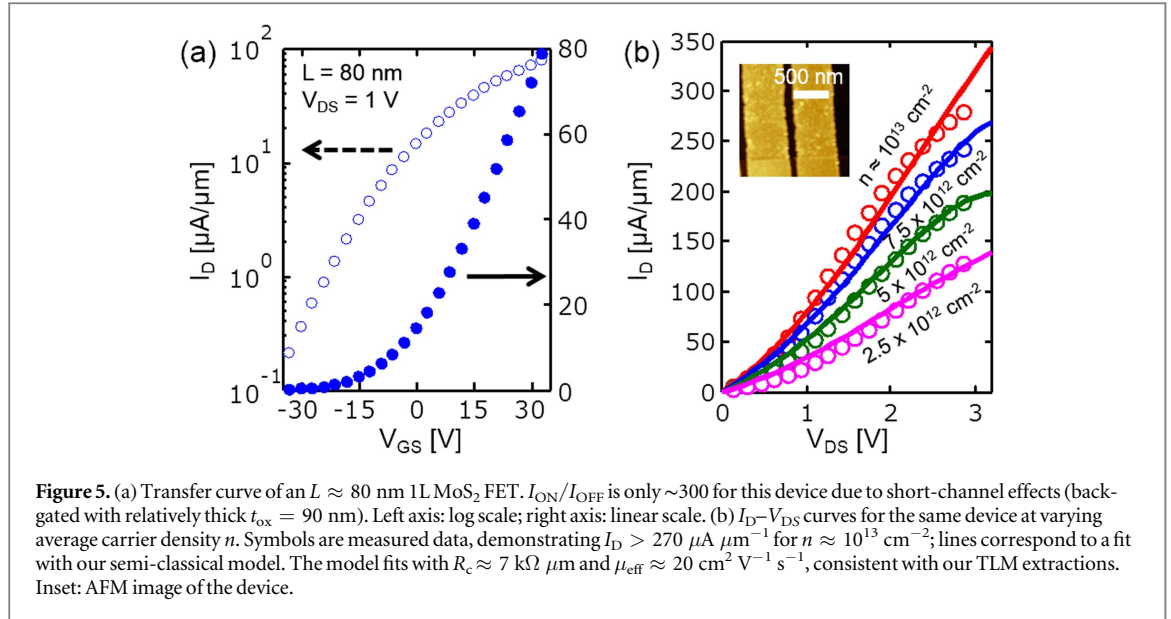
where $L_c = 1 \mu\text{m}$ is the length of the contacts and L_T is the current transfer length, i.e. the distance over which the current flowing in the MoS₂ drops to $1/e$ times the value injected at the contact edge. At 300 K, we extract $\rho_c \approx 10^{-5} \Omega \text{ cm}^2$, a value ~ 12 times higher than our best results for few-layer exfoliated MoS₂ at the same carrier density, $n = 4 \times 10^{12} \text{ cm}^{-2}$ [26]. As with R_c , we observe ρ_c to decrease with increasing T and V_{DS} in figure 4(b) due to enhanced thermionic and field emission, respectively. Interestingly, we do not see appreciable variation with n , as one might expect from a thinning of the Schottky barrier at the Au/MoS₂ interface, which would allow for enhanced field emission. Taken together, these two observations indicate that, while both thermionic and field emission play a role, the former is by far the dominant mechanism. This disparity should be exacerbated at

lower temperatures, as fewer carriers are able to thermionically surmount the barrier, and the ratio $\rho_c(V_{DS} = 0.1 \text{ V})/\rho_c(V_{DS} = 1.0 \text{ V})$ being 3 times larger at 80 K than at 300 K supports this conclusion. The weak yet observable variation of ρ_c with n for $T = 80$ K and $V_{DS} = 0.1$ V, where few carriers can make it over the barrier and field emission is suppressed, further supports this notion, as an increase in tunneling can then be more easily noticed. This is in contrast to our exfoliated few-layer devices [26], which have a shorter L_T (~ 40 nm) and ρ_c that clearly decreases with n .

We note that the approximation in equation (2) is only valid when $L_T \ll L_c$, in which case $\coth(L_c/L_T) \approx 1$, and we can rearrange to give

$$L_T \approx \sqrt{\frac{\rho_c}{R_{\text{SH}}}} \quad (3)$$

whereby we extract $L_T \approx 100 \text{ nm} \ll L_c$ at 300 K (shown in figure 4(c)), justifying our use of the approximation. As previously mentioned, both R_c and ρ_c decrease for higher V_{DS} due to increased field emission, especially at lower temperatures where thermionic emission is suppressed. This leads to L_T that is essentially constant with respect to n , but also decreases with increasing T and V_{DS} (shown in supplementary figure S6). This result suggests that contacts to 1L MoS₂



can be scaled to lengths as small as 100 nm before current crowding causes an increase in R_{c} .

Utilizing R_{SH} as given by the TLM fit slopes, the effective mobility can be calculated by

$$\mu_{\text{eff}} = (qnR_{\text{SH}})^{-1}, \quad (4)$$

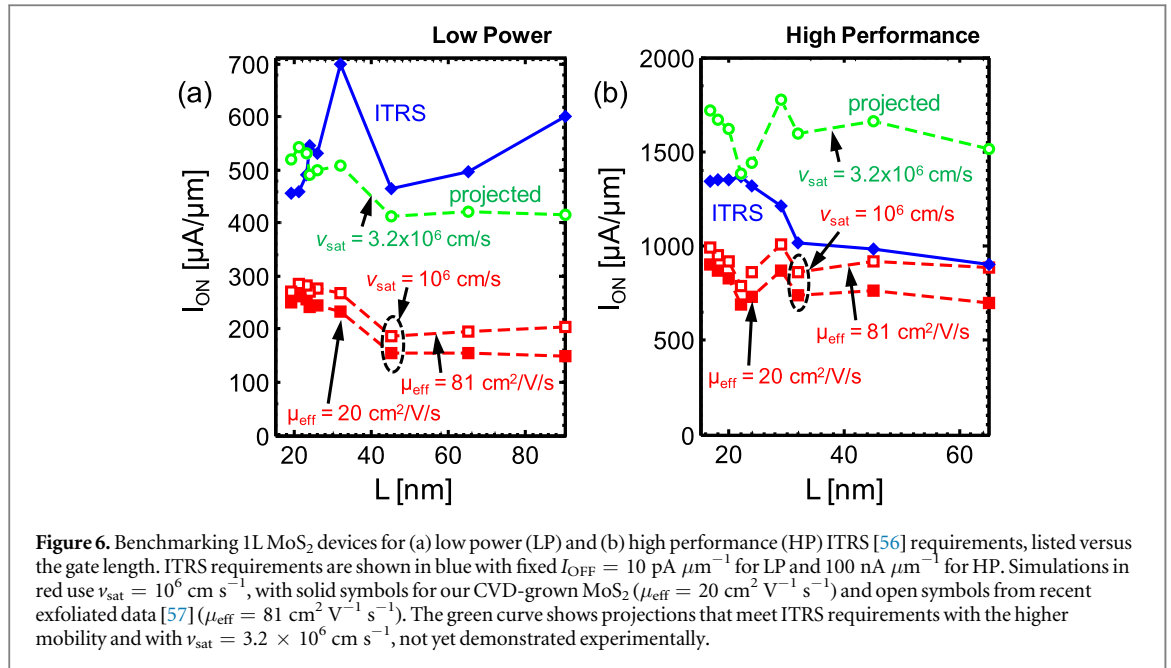
where q is the elementary charge and n is given by equation (1). As n increases and equation (1) better approximates the true charge in the channel, equation (4) approaches a constant lowest value, which we take to be the ‘true’ value for μ_{eff} in the technologically relevant high carrier density regime (see supplementary figure S6(b)).

We focus on *effective* mobility rather than field-effect mobility [$\mu_{\text{FE}} = L(\partial I_{\text{D}}/\partial V_{\text{GS}})/(WC_{\text{ox}}V_{\text{DS}})$] in this work because μ_{eff} is strictly a channel material parameter that is valid for all moderate values of n . In contrast, μ_{FE} is heavily dependent on V_{DS} and V_{GS} (due to the Schottky contacts), leading to a concept often referred to as a ‘peak mobility’ as a function of gate voltage [39, 48–50], and potentially resulting in under- or overestimations of the true channel mobility (see supplementary figures S7 and S8). The TLM analysis not only allows us to separate contributions by R_{c} and R_{SH} to R_{TOT} , but also allows for the direct use of μ_{eff} as a more reliable channel parameter in device models. In other words, the effective mobility is the more important figure of merit (rather than the field-effect mobility), linking materials, devices (via models, as done below), and system applications of TMDs. We also note that the μ_{eff} extracted here is a lower bound on the true band mobility [23] due to fast traps and impurities at the oxide interface, as opposed to mobility values that could be obtained from Hall measurements or from devices on a smooth, clean surface such as hexagonal boron nitride (h-BN) [51].

Analyzing extracted data for μ_{eff} versus T in figure 4(d) reveals μ_{eff} to be approximately constant near $\sim 28 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at low T . The lack of variation in μ_{eff} between 100 and 200 K suggests that these

values are limited by impurity scattering [52–54], possibly from particles or adsorbates deposited during device fabrication. Above 200 K, μ_{eff} is principally limited by optical phonon scattering and rolls off as $\sim T^{-\gamma}$ (where $\gamma \approx 1$), falling to a value of $20 \pm 3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at 300 K, comparable with the best CVD 1L devices reported so far [3–5, 19–21]. (Also see supplementary figure S9.) A larger temperature coefficient of mobility, γ , would be indicative of stronger (intrinsic) phonon scattering. As with our extractions of R_{c} , the uncertainty reflects 90% confidence intervals.

Finally, we wish to understand how the mobility and contact resistance rigorously studied thus far manifest themselves in very small devices. To this end, we fabricated a short-channel ($L \sim 80$ nm) FET on our 1L CVD-grown MoS₂ films, and we recorded the transfer characteristics shown in figure 5(a). At room temperature, we measure the highest current density reported to date ($\sim 270 \mu\text{A} \mu\text{m}^{-1}$ or 44 MA cm^{-2} , taking into account the appropriate 0.615 nm 1L thickness [36, 55]) for CVD-grown 1L MoS₂ FETs, as shown in figure 5(b). (An overview of other measurements for reported current density and mobility in 1L CVD MoS₂ is provided in supplementary figure S9.) The current drive is an important metric, because the intrinsic delay of a transistor is $\propto C_{\text{ox}}V_{\text{DD}}/I_{\text{ON}}$, where V_{DD} is the operating voltage. In other words, it is not the intrinsic mobility of the devices that affects the circuit delay, but the total drivable current, which might ultimately be limited by contacts or saturation velocity. Nonetheless, even at high carrier density ($n \sim 10^{13} \text{ cm}^{-2}$) we note sub-linear (i.e. Schottky-like) measured $I_{\text{D}}-V_{\text{DS}}$ up to $V_{\text{DS}} \sim 1$ V in figure 5(b), further demonstrating the need for reducing contact resistance for very short channel lengths. Values for μ_{eff} , R_{c} , and maximum I_{D} could also be further improved by suppressing the detrimental effects of the underlying oxide, i.e. by fabricating devices on h-BN, on oxides with higher phonon energies, or selecting



dielectrics to sufficiently screen charged impurities [54].

4. Simulation projections

Before concluding, we use simulations seeking to project how such short channel 1L MoS₂ FETs might behave with more idealized properties, i.e. with lower R_c and properly scaled insulators. To this end, we employ our physics-based device model (described elsewhere [27] and available online [28]) and first fit it against the measured data in figure 5(b), with $\mu_{\text{eff}} = 20\text{--}22 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and $R_c = 6\text{--}8 \text{ k}\Omega \mu\text{m}$, in good agreement with our TLM extractions described earlier. The model reveals that approximately two thirds of the applied V_{DS} is dropped at the contacts of the 80 nm device, further highlighting the need for contact engineering in such small devices. At higher drain voltage in figure 5(b), the model I_{D} begins to saturate not due to channel pinch-off, but rather due to carrier velocity saturation, which for these simulations was fit to a value of $v_{\text{sat}} = 7 \times 10^5 \text{ cm s}^{-1}$.

We then use our calibrated model [28] to predict the performance of such 1L semiconductors at scaled ITRS [56] technology nodes for HP and LP applications, in figure 6. We assume the *intrinsic* channel mobility extracted from experiments in this work and [57], but take the contact resistance ($R_c = 150\text{--}200 \Omega \mu\text{m}$) as required by the ITRS for HP and LP applications. To calculate the ON current we first iteratively adjust the flatband voltage through the gate workfunction to achieve the required OFF current, $I_{\text{OFF}} = 100 \text{ nA } \mu\text{m}^{-1}$ for HP and $10 \text{ pA } \mu\text{m}^{-1}$ for LP. We neglect the gate leakage current and the source-to-drain leakage which allows us to benchmark the maximum possible performance of the MoS₂ devices. We note that even the highly scaled devices considered in

figure 6 are fully in the diffusive transport regime (i.e. ballistic effects do not play a major role), because the electron mean free path in MoS₂ is only 1–3 nm (see figure S10) for mobility values between 20 and $80 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.

In figure 6 we consider two values for velocity saturation and two values for 1L MoS₂ mobility, as shown. The present state-of-the-art 1L MoS₂ (red curves, this work on CVD MoS₂ and that of [57] on exfoliated MoS₂) with $v_{\text{sat}} = 10^6 \text{ cm s}^{-1}$ fall short of the ITRS requirements for both HP and LP. However, this exercise highlights that the role of mobility is secondary, because at high lateral field I_{ON} is more strongly limited by v_{sat} . On the other hand, if the saturation velocity is increased to simulated projections [58, 59] of $v_{\text{sat}} = 3.2 \times 10^6 \text{ cm s}^{-1}$, we find that both the HP and the LP ITRS requirements could potentially be achieved using 1L MoS₂ (green curves) for the shorter channel devices (<20 nm), in agreement with recent quantum transport simulations [60].

It is relevant to inquire why ITRS specifications could be met with a v_{sat} that even optimistically remains lower than that of silicon. As illustrated in supplementary figure S11, the carrier confinement is different in 1L 2D materials than in typical semiconductors, such that the EOT could be smaller for 2D materials ($t_{\text{ox},2\text{D}} < t_{\text{ox},\text{Si}}$) even for the same physical oxide thickness. This allows 1L 2D materials to achieve higher carrier densities for similar oxide thickness and similar overdrive voltage, and thus higher I_{ON} even at lower carrier velocities, while meeting I_{OFF} requirements owing to their larger band gap. Consequently, future work on 2D transistors should focus not only on improving the contact resistance (as highlighted earlier), but also on understanding and improving the charge carrier drift velocities.

4. Conclusions

In summary, this work presents an in-depth analysis of CVD-grown 1L MoS₂ FETs with material characteristics comparable to those of exfoliated devices, achieving the highest current density reported to date ($\sim 270 \mu\text{A } \mu\text{m}^{-1}$ or 44 MA cm^{-2}). We show that the TLM approach provides rigorous estimates of both mobility and contact resistance, obtaining $R_c \approx 6.5 \text{ k}\Omega \mu\text{m}$ and $\rho_c \approx 10^{-5} \Omega \text{ cm}^2$ here, at room temperature and moderate carrier densities, which could be reduced further with contact engineering. We use simulations to match our experimental results and to provide insights into how 1L MoS₂ devices could behave when properly scaled down. It is revealed that v_{sat} plays a greater role than μ_{eff} in determining I_{ON} for aggressively scaled devices. Simulations also reveal that 1L MoS₂ could nearly meet ITRS requirements at sub-20 nm channel lengths, but further advancements in contact, dielectric, and carrier velocity engineering are still needed.

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Supporting information

Experimental setup of reported and optimized growth conditions, forward and backward I_D - V_{DS} sweeps showing minimal hysteresis, low-field I_D - V_{DS} sweeps showing linear behavior, plots of L_T versus n for various T and V_{DS} , extractions of field-effect mobility, simulations of extracted mobility values, summary plot of reported current density versus reported mobility in 1L CVD MoS₂, mean free path versus mobility, and illustrations of quantum confinement effects in 2D and bulk materials.

Author contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interests.

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SUPPLEMENTARY INFORMATION

Intrinsic Electrical Transport and Performance Projections of Synthetic Monolayer MoS₂ Devices

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A. Growth Details

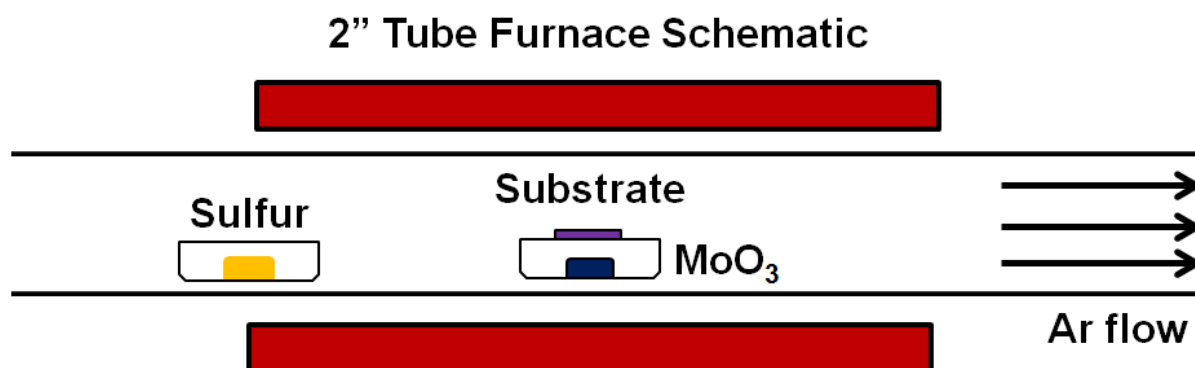


Figure S1. Diagram of experimental setup for large-grain 1L MoS₂ synthesis.

All growths are performed in a 2-inch inner diameter quartz tube, using a 2-inch Across International STF 1100 Tube Furnace connected to an Ebara A07 vacuum pump.

For the electrical data shown in this paper, experimental details are as follows. ~200 mg solid S was placed upstream in a quartz boat, and ~1 mg MoO₃ was placed in an alumina crucible liner at the center of the furnace, with 11 inches separating the precursors. A 90 nm SiO₂/Si substrate was treated with piranha solution (3:1 H₂SO₄:H₂O₂) for several hours before using a pipette to drop a single drop (~25 μ L) of 80 μ M perylene-3,4,9,10 tetracarboxylic acid tetrapotassium salt (PTAS) onto the substrate center. After drying the PTAS on a hot plate in air, the substrate was placed face-down on the crucible over the MoO₃. The growth recipe was:

- 1) Pump the tube to base pressure (~100 mTorr)
- 2) Ramp to 300 °C in 10 minutes while flowing 500 sccm Ar to reach 760 Torr
- 3) Anneal at 300 °C, 760 Torr for 5 minutes
- 4) Reduce the Ar flow to 10 sccm, ramp to 850 °C in 15 minutes and hold for 15 minutes
- 5) Allow the furnace to cool to <600 °C before opening the hatch for rapid cooling

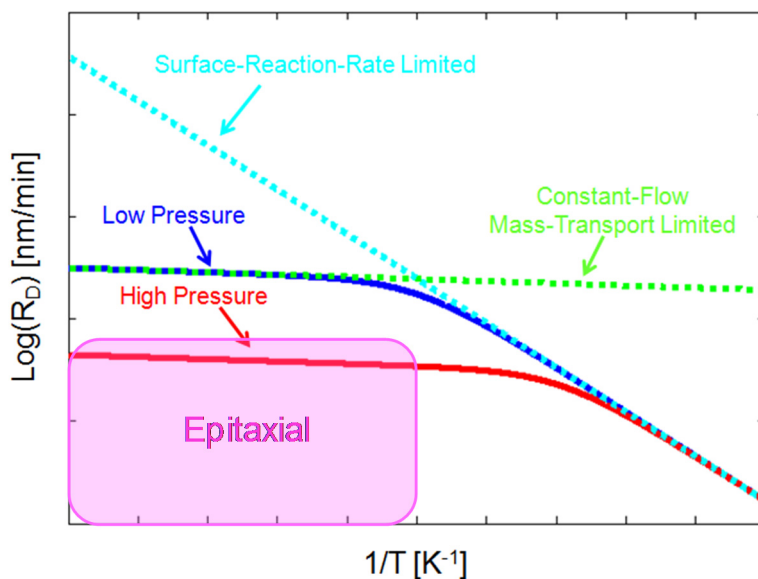


Figure S2. Representative plot of (constant-flow) CVD deposition rate, R_D , vs. inverse temperature, $1/T$.

In order for CVD films to grow epitaxially, the surface diffusion length, $L_D \propto (R_D)^{-1/2} \exp(-E_A/k_B T)$, of a given species must be maximized. This can be achieved by decreasing the deposition rate, R_D , and/or increasing T . In general, $R_D = k_s h_g (k_s + h_g)^{-1} \times (C_G/N)$, where C_G is the gas-phase concentration of reactive species, N is the number of species per unit volume of the deposited film ($1.9 \times 10^{22} \text{ cm}^{-3}$ for MoS_2), $h_g \propto (P_{\text{tot}})^{-1}$ is the mass transfer coefficient (inversely proportional to total system pressure), and $k_s \propto \exp(-E_A/k_B T)$ is the surface reaction rate (very strongly dependent on T) [1].

From the equation for R_D , it is evident that, for given values of C_G and N , R_D will be limited by either k_s or h_g . For best process control, it is easiest to operate in a mass-transport limited regime, and to this end increasing T is desirable. Additionally, increasing the total ambient pressure of the system greatly decreases R_D when growth is mass-transport limited, and so increased pressure (in this case, ~ 760 Torr) is also advantageous. The biggest difference between the ideal case shown in Figure S2 and the CVD processes employed in this work is the use of solid precursors, which causes C_G to be a function of precursor mass, temperature, pressure, and even time. Thus the exact amount of solid precursors must be simultaneously tuned with growth conditions to achieve uniform 1L deposition across large areas. Finally, the increased pressure causes the mean free path of gaseous reactive species, $\lambda \propto (k_B T/P_{\text{tot}})$ to be greatly reduced. Thus the solid precursor must be evenly distributed directly underneath the growth substrate to mimic showerhead injectors used for APCVD (atmospheric pressure CVD) with gaseous precursors.

With these points in mind, a more optimized growth recipe that allows for continuous mostly monolayer ($\sim 90\%$ 1L by area while maintaining large single crystal sizes, as in Fig. 1 of the main text) was established after the device fabrication. (Electrical data for these growths will be provided in a future manuscript.) The experimental setup for this recipe involved separating the precursors by ~ 10 inches, reducing the MoO_3 amount, and using hydrophobic SiO_2/Si treated with HMDS to

ensure that PTAS droplets consume as little area as possible. 20 - 30 μL of 100 μM PTAS is placed in 2 - 5 μL droplets around the edges of the growth substrate (seen as “coffee ring” circles after growth, in Fig. 1a of the main text), and 0.2 - 0.8 mg of MoO_3 are used to tailor the growths to achieve large individual MoS_2 crystals or a continuous film, respectively. This recipe is:

- 1) Pump the tube to base pressure (~ 100 mTorr)
- 2) Flush the tube with 1500 sccm Ar and then close the butterfly valve to reach 760 Torr
- 3) Ramp to 400 $^\circ\text{C}$ in 10 minutes and reduce the Ar flow to 30 sccm*
- 4) Ramp to 850 $^\circ\text{C}$ in 20 minutes and hold for 15 minutes
- 5) Allow the furnace to cool to 650 $^\circ\text{C}$ before opening the hatch for rapid cooling

*note: 30 sccm in a 2-inch tube corresponds to 7.5 sccm in a 1-inch tube.

The PTAS seeding layer is essential for obtaining large-area MoS_2 growth on the SiO_2 surface. Similar to [2], only islands of small (< 500 nm) MoS_2 particles could typically be grown on SiO_2 substrates at any temperature without the use of PTAS.

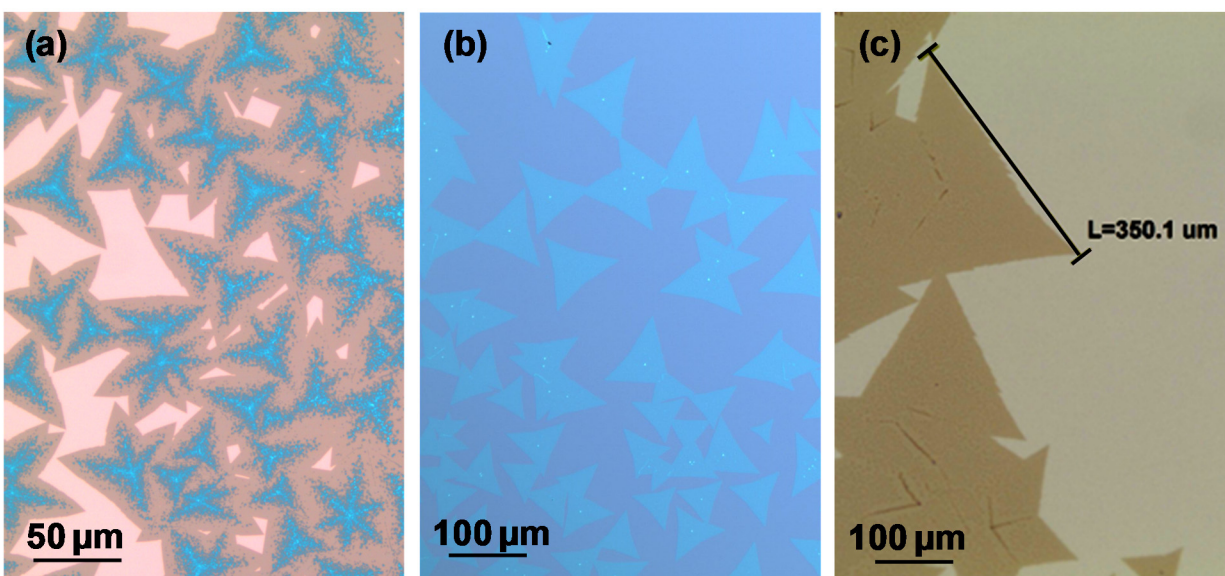


Figure S3 Optical images of different MoS_2 growths. (a) The growth that yielded the devices discussed in the main text, grown on 90 nm SiO_2 on Si. (All devices were fabricated on the monolayer regions.) (b) The optimized growth that allows for very large, all monolayer MoS_2 triangles similar to Fig. 1a, but grown on 300 nm SiO_2 . (c) Edge of a continuous MoS_2 film from a tailored growth showing 1L single-grain sizes in excess of 350 μm on an edge, grown on 30 nm SiO_2 on Si. Darker regions in continuous films are small bilayer regions that can appear at highly-misoriented grain boundaries or when the size of the individual crystals exceeds the surface diffusion length for the given growth conditions.

B. Additional Electrical Data and Transfer Length Calculations

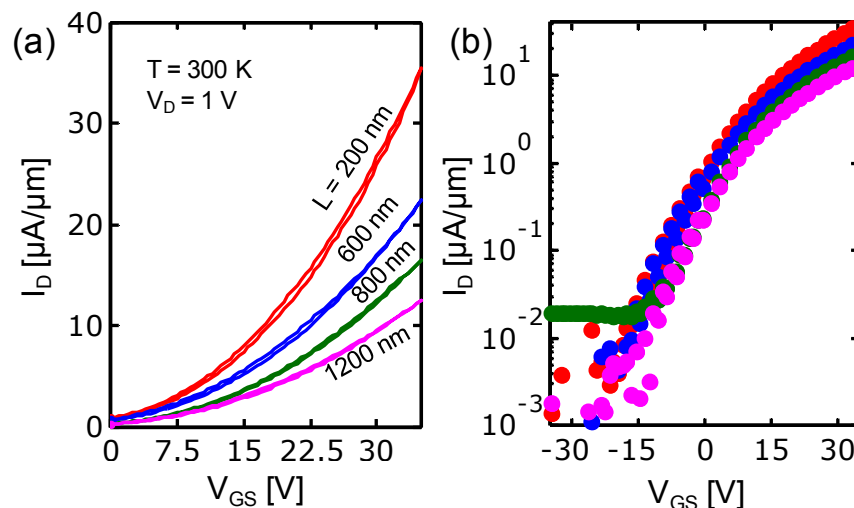


Figure S4. (a) Forward and backward I_D - V_{GS} sweeps demonstrating very little hysteresis of our devices in vacuum. (b) Measured data for the same transfer curves shown in (a) plotted in log scale, showing $I_{ON}/I_{OFF} \geq 10^4$ (partly limited here by the measurement range of the Keithley 4200 semiconductor parameter analyzer).

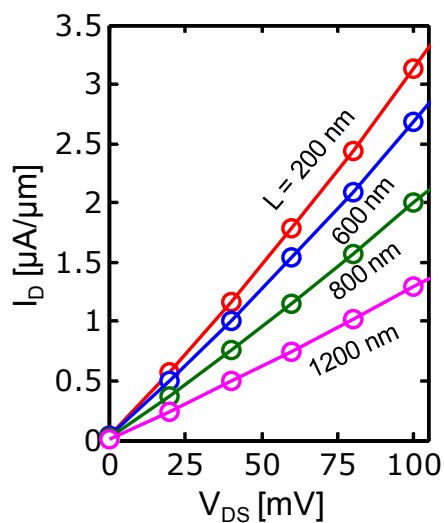


Figure S5. Low-field I_D - V_{DS} sweeps are linear but do not necessarily indicate Ohmic contacts in terms of band alignment at the contacts. As extracted in the main text, there is still a non-negligible contact resistance due to a Schottky barrier at the Au-MoS₂ interface.

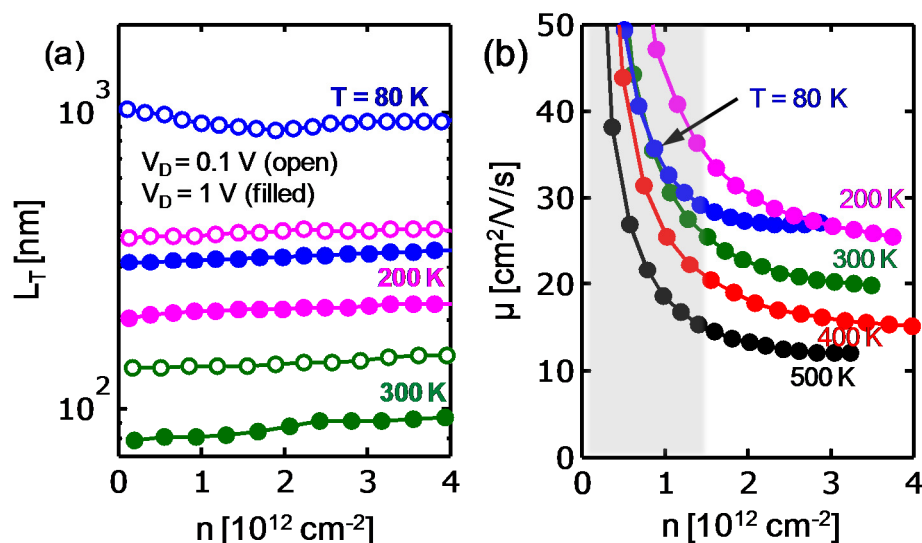


Figure S6. (a) Contact transfer length vs. carrier density in log scale. The trend is similar to that in Fig. 4b of the main text due to the dependence of L_T on ρC in Equation 3. (b) μ_{eff} vs. n for various T . The gray shaded region indicates μ_{eff} with errors $\geq 30\%$ for low n due to the assumed linear inversion charge model.

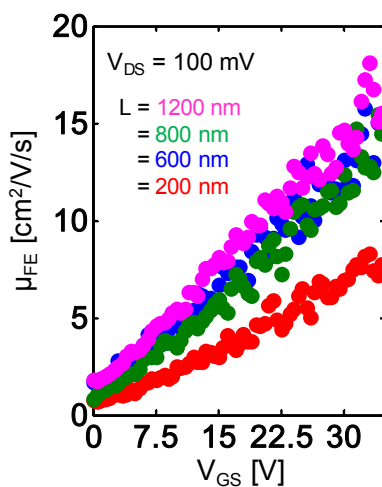


Figure S7. Field-effect mobility extractions for the same devices in Fig. 3a of the main text, here with $V_{\text{DS}} = 0.1 \text{ V}$. Although the phenomenon of "peak mobility" is not exhibited in our devices, for all values of V_{GS} , $\mu_{\text{FE}} < \mu_{\text{eff}}$, similar to the simulations in Fig. S8b. Note that shorter channel devices exhibit lower μ_{FE} due to the larger contribution of R_C to total device resistance.

C. Simulations of Extracted Mobility Values

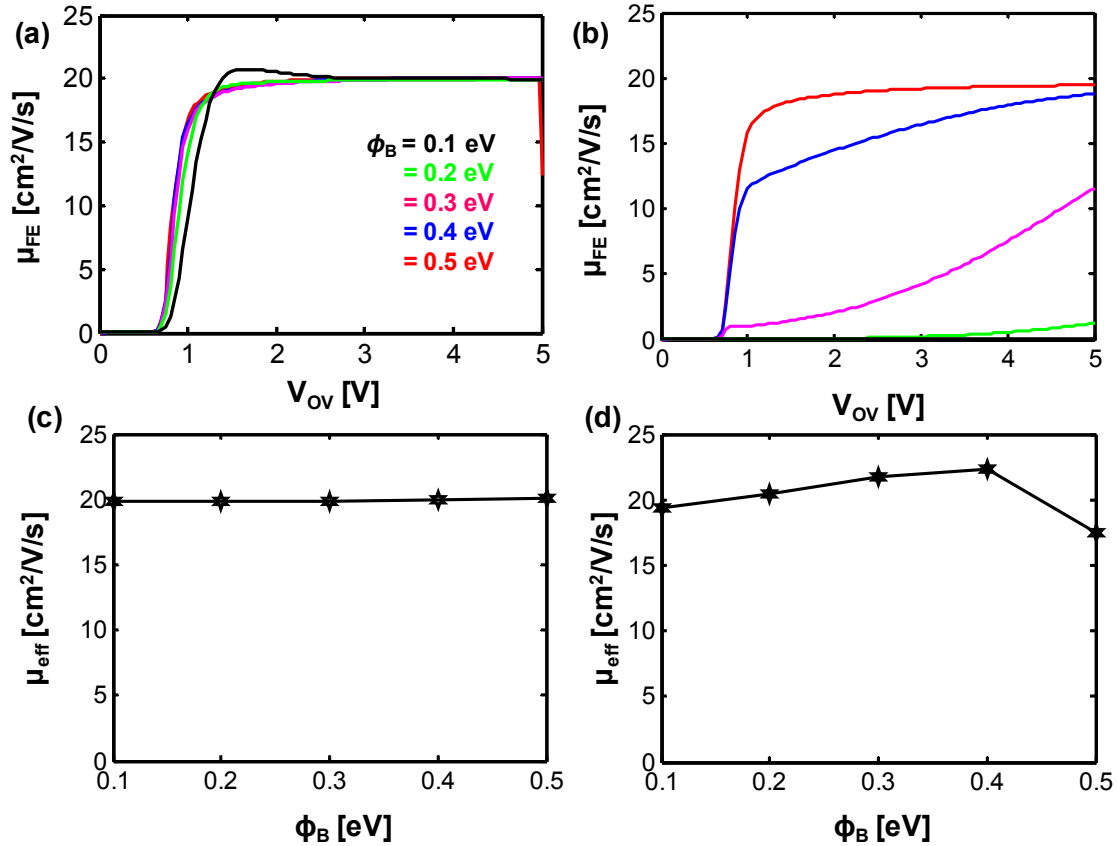


Figure S8. (a) and (b) Sentaurus simulated *field-effect mobility* extractions plotted against overdrive voltage ($V_{OV} = V_{GS} - V_T$) for varying Schottky barrier heights and tunneling masses of $0.01m_0$ and $1.0m_0$, respectively. $\mu_0 = 20 \text{ cm}^2/\text{V/s}$ and $V_{DS} = 0.1 \text{ V}$ for all simulations. Both over- and under-estimation of the “true” mobility can be seen for various contact resistance parameters. (c) and (d) Sentaurus simulated *effective mobility* extractions from TLM structures plotted against varying Schottky barrier heights for tunneling masses of $0.01m_0$ and $1.0m_0$, respectively. $\mu_0 = 20 \text{ cm}^2/\text{V/s}$ and $V_{DS} = 1.0 \text{ V}$ for all simulations. The “true” channel mobility is extracted for all combinations of m_{tun} and ϕ_B .

D. Brief History of Electrical Results Reported for Synthetic Monolayer MoS₂

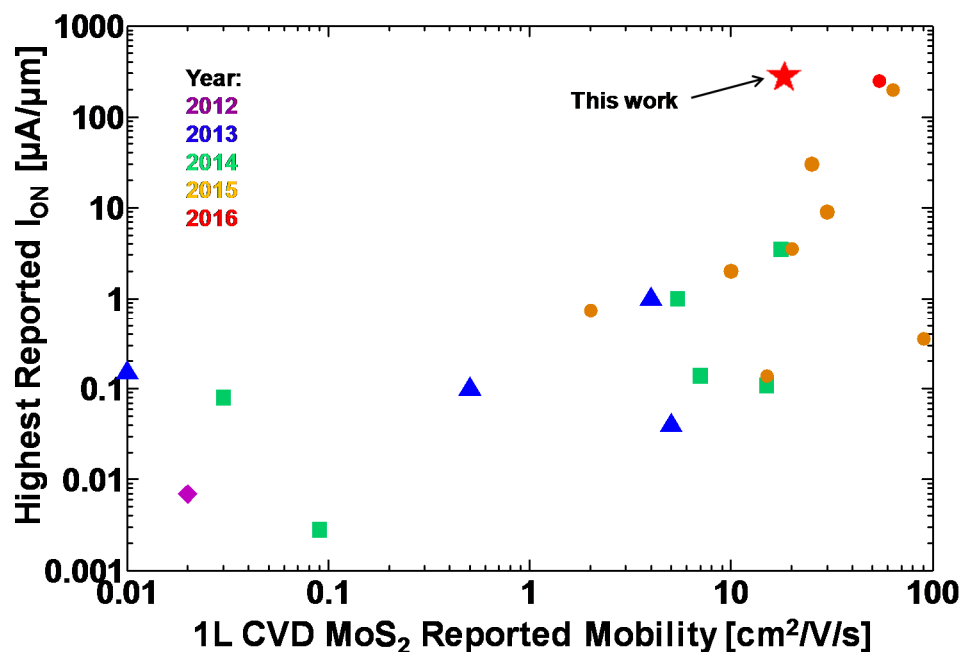


Figure S9. Historical plot of 1L CVD MoS₂ devices with highest reported drive currents and reported mobility values [2-22]. The type of mobility value reported varies by source, and this plot includes two-terminal and four-terminal field-effect mobility, two-terminal field-effect mobility with contact resistance estimated and subtracted, Y-function method [23], effective mobility extracted from TLM devices (this work, generally assumed to be more reliable), and mobility fit to velocity saturation models. References for these data are given in the Supplement References section below, in order of ascending mobility.

E. Estimation of the mean free path (λ_{MF}) in MoS₂

We can estimate the mean free path as $\lambda_{MF} = v_{2D}\tau_C$, where $v_{2D} = (\pi k_B T / 2m_{eff})^{1/2}$ is the average thermal velocity of electrons and $\tau_C = \mu_{eff} m_{eff} / q$ is the average collision time for carriers. Here, k_B is the Boltzmann constant, T is the average device temperature, μ_{eff} is the effective mobility at the temperature T , q is the elementary charge, and m_{eff} is the in-plane carrier effective mass. For electrons in monolayer MoS₂, $m_{eff} = 0.48m_0$ where m_0 is the mass of free electron.

As can be seen from Fig. S10, the mean free path for electrons is well below the channel lengths of the MoS₂ studied in this paper ($\lambda_{MF} \sim 1$ to 3 nm for μ_{eff} of 20 to 80 cm²/V/s). The low mean free path for electrons, therefore, justifies the use of semi-classical transport for the model used for MoS₂ performance projections.

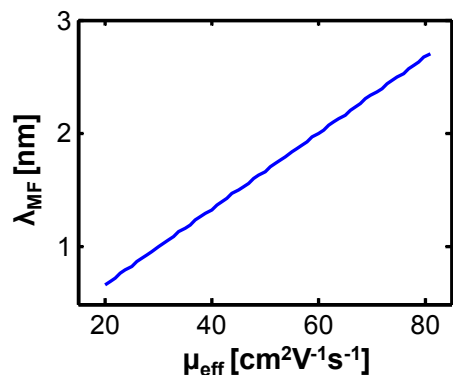


Figure S10: Estimated electron mean free path (λ_{MF}) MoS₂ vs. electron mobility (μ_{eff}).

F. Carrier confinement in 2D and 3D MOSFETs

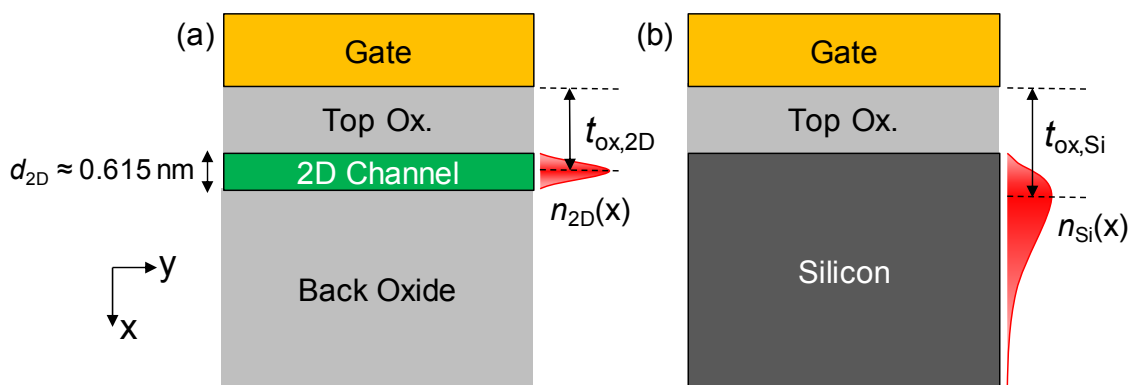


Figure S11: Schematic showing the effect of quantum confinement in MOSFET channel with: (a) monolayer MoS₂ and (b) traditional bulk materials like silicon. The red curve shows the carrier density as a function of the channel depth (x). In 2D monolayer channels, the effective oxide thickness $t_{\text{ox},2\text{D}} < t_{\text{ox},\text{Si}}$ for similar oxide physical thickness and gate voltage overdrive.

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