ACS APPLIED MATERIALS & INTERFACES

www.acsami.org

Research Article

Improved Current Density and Contact Resistance in Bilayer $MoSe_2$ Field Effect Transistors by AlO_x Capping

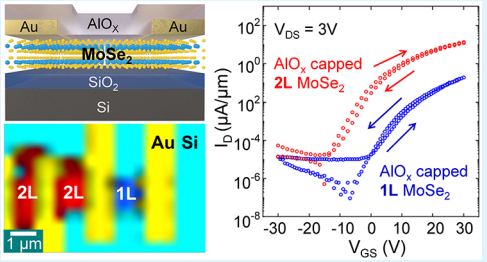
Divya Somvanshi,[⊥] Emanuel Ber,[⊥] Connor S. Bailey, Eric Pop, and Eilam Yalon*

Cite This: *ACS Appl. Mater. Interfaces* 2020, 12, 36355−36361

Read Online

ACCESS | Metrics & More | Article Recommendations | Supporting Information

ABSTRACT: Atomically thin semiconductors are of interest for future electronics applications, and much attention has been given to monolayer (1L) sulfides, such as MoS_2, grown by chemical vapor deposition (CVD). However, reports on the electrical properties of CVD-grown selenides, and $MoSe_2$ in particular, are scarce. Here, we compare the electrical properties of 1L and bilayer (2L) $MoSe_2$ grown by CVD and capped by sub-stoichiometric AlO_x. The 2L channels exhibit ∼20× lower contact resistance (R_C) and ∼30× larger current density compared with 1L channels. R_C is further reduced by >5× with AlO_x capping, which enables improved transistor current density. Overall, 2L AlO_x-capped $MoSe_2$ transistors (with ∼500 nm channel length) achieve improved current density (∼65 μA/μm at V_{DS} = 4 V), a good I_{on}/I_{off} ratio of >10^6, and an R_C of ∼60 kΩ·μm. The weaker performance of 1L devices is due to their sensitivity to processing and ambient. Our results suggest that 2L (or few layers) is preferable to 1L for improved electronic properties in applications that do not require a direct band gap, which is a key finding for future two-dimensional electronics.



KEYWORDS: *molybdenum diselenide, monolayer, bilayer, contact resistance, field-effect transistor, oxide capping, doping, 2D semiconductors*

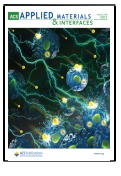
1. INTRODUCTION

Reducing contact resistance and finding industry-compatible doping methods are two major challenges for the fabrication of electronic devices based on two-dimensional (2D) materials.[1−3] These challenges are tightly interrelated because higher doping concentration can reduce contact resistance. Phase engineering of contacts,[4] ultrahigh vacuum metal deposition,[5−7] transfer of contacts onto 2D materials,[6,8,9] and edge contacts[10−12] have been suggested as means of lowering contact resistance. Deposition of substoichiometric oxides was demonstrated for electron doping and contact resistance reduction in MoS_2 monolayers (1Ls),[13,14] yet further reduction by an order of magnitude needs to be achieved for this technology to prove competitive with silicon-based devices.[15,16]

There have been extensive efforts invested toward the fabrication of good 1L devices. Interuniversity Microelectronics Centre[17] has recently reported 300 mm wafer scale 1L WS_2 field effect transistors (FETs) with a current density of ∼10 μA/μm and mobility of few cm^2 V^{-1} s^{-1}. In addition, Smithe et al.[18] showed low electrical variability in CVD-grown 1L MoS_2 despite the presence of bilayers (2Ls) because of small 1L/2L conduction band offsets. However, to date, there is no clear-cut compelling argument for the use of 1L semiconductors, as opposed to 2L, trilayer (3L), or few layers (FL) for optimized device behavior. Naturally, 1L transistor channels have better electrostatic control; however, FL devices can achieve better contact resistance and mobility and carry more current.[19−22] Moreover, the evaporation of metal contacts can damage the top layer of the target material.[23] Edge contacts[10−12] can be significantly improved in FL devices, thanks to the larger cross sectional area of charge injection. It is clear, therefore, that it would be interesting to investigate 2L (or FL) devices, as their benefits compared to 1L devices may be the key to achieving the sought-after order of magnitude improvement in contact resistance and current density, while preserving the superior electrostatics.

$MoSe_2$ is potentially a good candidate for low power electronic applications with a direct electronic (optical) band gap of ∼2 eV (∼1.5 eV) in 1L and ∼1.1 eV indirect band gap in the bulk.[24−29] Furthermore, its ambipolar behavior coupled with relatively high electron and hole mobilities (200 and 150 cm^2 V^{-1} s^{-1}, respectively, in multilayer films)[19,30−33] is promising for CMOS applications. Still, $MoSe_2$ remains relatively unexplored in the device community,[34] likely because of more challenging growth of large-area high-quality materials as compared with MoS_2 and WS_2.[19,35−37] However, Li et al.[19] have recently demonstrated controlled layer-number (1L and FL) large area synthesis of crystalline $MoSe_2$, further advancing

Received: May 25, 2020
Accepted: July 17, 2020
Published: July 17, 2020



https://dx.doi.org/10.1021/acsami.0c09541
ACS Appl. Mater. Interfaces 2020, 12, 36355−36361

the possibility of the 1L *versus* FL debate. Therefore, comparing the electrical properties of FL and 1L $MoSe_2$ becomes relevant and essential for the purpose of device optimization and is the centerpiece of our research.

In this work, we compare the electrical characteristics of CVD-grown 1L *versus* 2L $MoSe_2$ FETs. We use Raman spectroscopy maps to identify the number of layers (1L or 2L) of transistor channels and apply AlO_x and N_2 annealing for passivation and electron doping of both types of devices. Our AlO_x-capped 2L devices achieve a record-high current density for atomically thin $MoSe_2$ of ~65 μA/μm, with an $I_{on}/I_{off} > 10^6$ and R_C of ~60 k$\Omega\cdot\mu$m.[30,34,38−40] These results represent ~20× improvement in R_C and ~30× enhanced current density compared to our (AlO_x-capped) 1L devices. The AlO_x doping effect aligns well with previously reported data for 1L and FL MoS_2 and ReS_2 encapsulation.[14,41] Our findings suggest that more research focus should be dedicated to exploring synthetic FL (likely 2L or 3L) transistor channels and contacts for future 2D electronics.

2. RESULTS AND DISCUSSION

2.1. Material Characterization and Device Structure.

Figure 1 shows an optical image of our 1L $MoSe_2$, a schematic diagram of the fabricated device, Raman, and photoluminescence (PL) spectra of the $MoSe_2$ 1L with and without AlO_x capping. The $MoSe_2$ film was deposited on SiO_2/Si substrates by CVD, more details about the process are found in Section S1. The optical image in Figure 1a consists mostly of 1L $MoSe_2$ triangles of size ~10−20 μm, although some 2L regions (~1−2 μm) are also present. To evaluate the electrical properties of 1L and 2L $MoSe_2$, we fabricated FETs on SiO_2 (t_{ox} = 90 nm) on p^{++} Si substrates, which serve as back gates. A schematic diagram of the as-fabricated 1L FET is shown in Figure 1b. We capped the devices with ~20 nm substoichiometric aluminum oxide (AlO_x) by atomic layer deposition (ALD) for encapsulation and electron doping.[14,41] Fabrication details for the $MoSe_2$ devices and AlO_x capping are given in the Methods section.

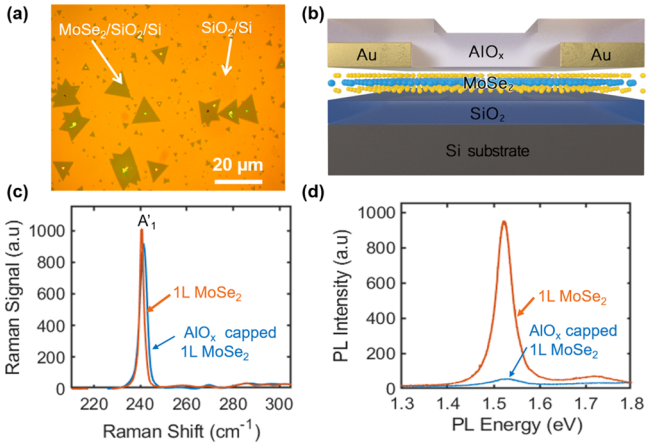


Figure 1. Material characterization and device structure. (a) Optical image of CVD-grown 1L $MoSe_2$. The orange colored area is the bare SiO_2/Si substrate, and the green triangles are 1L $MoSe_2$ on SiO_2/Si substrates. Some 2Ls and FLs are present at the nucleation centers. (b) Schematics of the $MoSe_2$ FET (capped by ~20 nm AlO_x) with Au source/drain electrodes on t_{ox} = 90 nm SiO_2 with a p^{++} Si substrate, which serves as a global back gate. (c) Raman spectra of 1L $MoSe_2$ before (orange) and after (blue) AlO_x capping. Blue shift (~1.15 cm^{-1}) and broadening in the A_1' Raman mode are observed, which indicate induced electron doping. (d) PL measurement of $MoSe_2$ before and after AlO_x capping. 1L $MoSe_2$ shows a strong peak at 1.52 eV with high intensity, displaying the direct optical band gap of 1L $MoSe_2$. After AlO_x capping, a decrease in PL intensity and broadening of ~25 meV is observed without change in the peak position.

We use Raman and PL spectroscopy (532 nm) for optical characterization of $MoSe_2$ with and without AlO_x capping. The measured Raman spectra of bare (orange) and AlO_x-capped (blue) 1L $MoSe_2$ are displayed in Figure 1c. The A_1' Raman active mode (out-of-plane vibration of Se atoms) is observed at 240.2 cm^{-1} for 1L $MoSe_2$, which is consistent with previous reports on the $MoSe_2$1L.[42−45] We note that A_1' notation of this Raman mode is valid for 1L and odd number of (few) layers, whereas it is labeled A_{1g} for bulk and even number of layers.[7,46,47] After capping the 1L $MoSe_2$ by AlO_x, a blue shift of ~1.15 cm^{-1} and broadening in the A_1' Raman mode are observed, demonstrating strong doping dependence, as previously reported for 1L MoS_2.[48] The room temperature PL spectrum of bare 1L $MoSe_2$ shows a strong emission peak at 1.52 eV with a full-width at half-maximum (fwhm) of ~50 meV, as shown in Figure 1d. This is attributed to the optical band gap of 1L $MoSe_2$ at the K high symmetry point of the Brillouin zone[38,44,49] (we note that the electronic gap of 1L $MoSe_2$ is larger by ~0.5 eV, the exciton binding energy[27,28]). After the AlO_x capping, however, the PL intensity is quenched and broadened (fwhm ~ 75 meV), while the peak position remains constant. This is attributed to the creation of defect states and the enhanced recombination rate in 1L $MoSe_2$ due to AlO_x capping.[14]

2.2. Raman Spectroscopy and Optical Microscopy Characterization of 1L and 2L $MoSe_2$ Devices.

Figure 2a,b shows the Raman spectral comparison between 1L and 2L

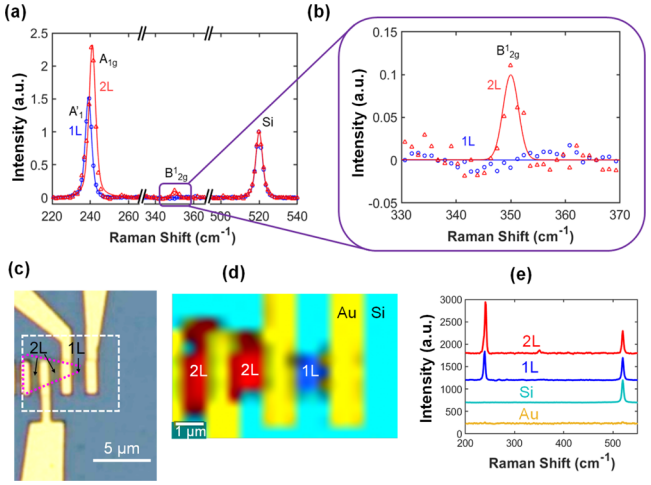


Figure 2. 1L and 2L Raman spectra and transistor channel Raman maps. (a) Overlaid Raman spectra of 1L and 2L $MoSe_2$, showing a red shift of ~1 cm^{-1} from A_1' in 1L to the A_{1g} mode in 2L. A low intensity B_{2g}^1 Raman mode is present only for 2L $MoSe_2$. (b) Enlarged B_{2g}^1 Raman mode for 1L and 2L $MoSe_2$, showing no peak for 1L $MoSe_2$, whereas a clear peak is observed for 2L $MoSe_2$. (c) Optical image of 1L and 2L $MoSe_2$ transistor channels with the area used for Raman mapping highlighted. (d) Raman intensity map of 1L and 2L $MoSe_2$ transistor channels (blue and red) with the gold electrode (yellow) and SiO_2/Si substrates (turquoise). (e) Comparison of Raman spectra that correspond to Au, Si, 1L, and 2L $MoSe_2$ channels shown in (d). The intensities in (a), (b), and (e) are normalized by the Si peak.

https://dx.doi.org/10.1021/acsami.0c09541
ACS Appl. Mater. Interfaces 2020, 12, 36355−36361

$MoSe_2$. The distinction between layer numbers is made clear by the characteristic ~1 cm^{-1} red shift from the A_1' peak in 1L $MoSe_2$ to the A_{1g} peak in 2L $MoSe_2$[24,50] and is further confirmed by the B_{2g}^1 peak that is present only for 2L $MoSe_2$.[24,36,43] Figure 2c shows the optical image of several FETs fabricated on the same $MoSe_2$ sheet, and Figure 2d overlays the Raman mapping based on the 1L, 2L, Au, and Si spectra on top of Figure 2c. Figure 2e compares the different spectra used for Raman mapping. Figure 2c shows fabricated FETs based on 1L and 2L channels distinctively, which can be used to compare their electrical characteristics.

2.3. Electrical Characteristics of 1L and 2L $MoSe_2$ FETs and AlO_x Capping. We analyze the electrical characteristics of bare 1L and 2L $MoSe_2$ FETs and the effect of AlO_x capping on the performance of the fabricated devices. It is noted that the reports available on the electrical properties of $MoSe_2$ are limited; mostly, reported studies are focused on either multilayer[30,31,33,39] or 1L[19,38,40] $MoSe_2$ FETs. Little attention has been given to the electrical characteristics of 2L $MoSe_2$ FET devices.[19]

Figure 3 compares dual sweep linear and logarithmic (log) scale DC transfer characteristics of 1L (orange) and 2L (black) $MoSe_2$ FETs measured in air at V_{DS} = 1 V. Note that all $I-V$ measurements presented in this work were performed at room temperature with forward and backward sweeps. The bare 1L $MoSe_2$ FET exhibits typical n-FET behavior with a drain current (I_D) of ~0.6 nA/μm at positive gate voltage (V_{GS}) = 40 V, and the on−off current ratio (I_{on}/I_{off}) is ~10^2. Such poor performance is consistent with previous reports.[36,40] The 2L $MoSe_2$ FET shows ambipolar behavior, an I_D of ~6.5 nA/μm at V_{GS} = 40 V with an I_{on}/I_{off} of ~10^3 and an I_D of ~0.1 nA/μm at V_{GS} = −40 V. Li et al. observed similar transport behavior of 2L $MoSe_2$ devices.[19] The uncapped 1L and 2L $MoSe_2$ FETs did not exhibit improvements in their current density following annealing in N_2 ambient at 250 °C for 30 min.

Next, the devices were capped by AlO_x to improve their electrical characteristics. Figure S1 compares the transfer characteristics of the 1L $MoSe_2$ FET before and after AlO_x capping, demonstrating a less significant change in I_{on}/I_{off} and I_D with some hysteresis. Figure 3b shows transfer characteristics of uncapped and AlO_x-capped 2L $MoSe_2$ devices, and significant improvement in ambipolar characteristics is observed. The capped 2L devices show an improved I_{on}/I_{off} of ~10^5, a negative shift in threshold voltage (V_T) of ~−2.1 V across 90 nm SiO_2 gate dielectric, and a field-effect mobility (μ_{FE}) of ~2 $cm^2\ V^{-1}\ s^{-1}$ (compared to ~0.3 $cm^2\ V^{-1}\ s^{-1}$ for uncapped devices). The increased I_D and lower hysteresis with AlO_x capping are consistent with those of AlO_x-encapsulated MoS_2 devices reported in the literature.[14,41,51]

Figure 3c,d shows the hole and electron current output characteristics of 2L $MoSe_2$ FETs after AlO_x capping. A nonlinear output characteristic is observed because of the presence of a Schottky barrier at the source and drain contacts.[52−55] I_D increases with the increase in positive and negative V_{GS} from 10 to 40 V, which also confirms the ambipolar characteristics of the device. It is observed that the performance significantly improves after AlO_x capping, which is attributed to the removal of unintentional adsorbents in the transistor channel, thanks to passivation by oxide capping.[41]

2.4. High-Performance AlO_x-Doped 2L $MoSe_2$ FETs. After AlO_x capping, annealing is performed in N_2 ambient at 200 °C for 40 min. Figure 4a compares transfer characteristics of the AlO_x-capped 2L $MoSe_2$ FET before (blue) and after (red) N_2 annealing. A negative shift in V_T of ~−7.5 V is observed after annealing, which indicates increased electron concentration. Both electron and hole currents are enhanced with an electron mobility μ_{FE} of ~4 $cm^2\ V^{-1}\ s^{-1}$. The ON current increases by more than ~25%, with an improved I_{on}/I_{off} of ~10^6. Figure S1 compares the transfer characteristics of the 1L $MoSe_2$ FET before and after N_2 annealing, exhibiting similar trends for V_T, although I_{on}/I_{off} does not change significantly. The high I_{on}/I_{off} ratio after N_2 annealing can be partially attributed to the improvement in I_D that is likely enabled by the lower resistance Au/2L contacts compared to

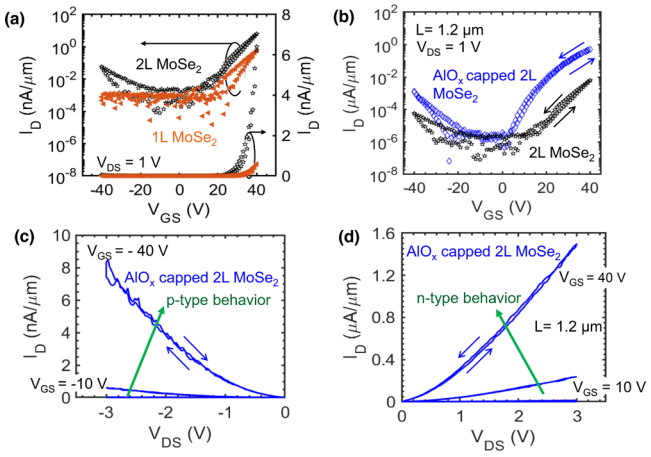


Figure 3. Electrical characteristics of 1L and 2L $MoSe_2$ FETs. (a) Transfer characteristics of 1L and 2L $MoSe_2$ FETs at V_{DS} = 1 V, measured in air. A typical n-FET behavior is observed for 1L $MoSe_2$, whereas an ambipolar behavior is observed for 2L $MoSe_2$ with dominant I_D at positive V_{GS}. (b) Transfer characteristics of the 2L $MoSe_2$ FET with (blue) and without (black) AlO_x capping. An increase in I_{on}, higher I_{on}/I_{off} (~10^5), and reduced hysteresis are observed for the capped devices. (c) Hole and (d) electron current output characteristics of the 2L $MoSe_2$ FET with AlO_x capping.

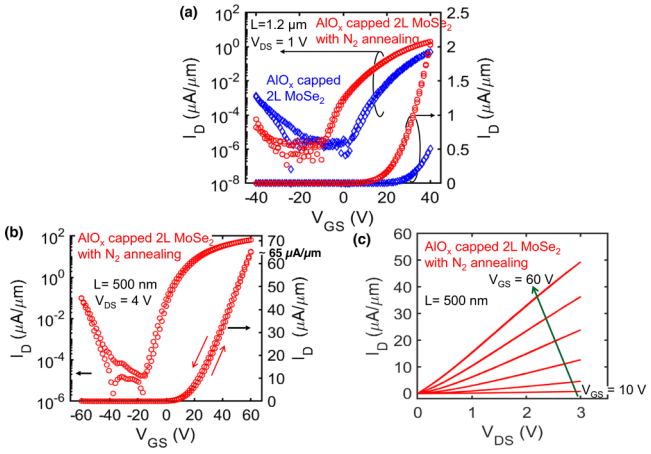


Figure 4. AlO_x doping and improved performance of 2L $MoSe_2$. (a) Comparison of transfer (linear and log scale) characteristics before (blue) and after (red) N_2 annealing. An increase in I_{on}, an improved I_{on}/I_{off} ratio of > 10^6, and a threshold voltage shift of ΔV_T = −7.5 V are observed, which indicate induced electron doping. (b) Transfer and (c) output characteristics of a 500 nm-long AlO_x-capped 2L $MoSe_2$ FET after N_2 annealing at 200 °C for 40 min. The transfer curve shows a peak current density of ~65 μA/μm at V_{DS} = 4 V, and the output curve shows linear I_D-V_{DS} relation.

https://dx.doi.org/10.1021/acsami.0c09541
ACS Appl. Mater. Interfaces 2020, 12, 36355−36361

Au/1L $MoSe_2$ because of the lower Schottky barrier height and reduced surface damage from contact evaporation.[21,22,56]

Because the devices were measured in air, the role of AlO_x capping is twofold: it passivates the atomically thin channel from the air ambient and it may also increase the electron density. The effects of AlO_x capping and annealing on our $MoSe_2$ devices can be explained in a similar manner to the recent reports on MoS_2 and ReS_2 FETs.[14,41] Based on internal photoemission measurements of 1L $MoSe_2$,[57] its band alignment with AlO_x allows for electron doping, namely, its conduction band minima lie below donor-type defects in AlO_x.[41]

Figure 4b shows the transfer characteristics of the AlO_x-capped 2L $MoSe_2$ FET (channel length L = 500 nm) after N_2 annealing, reaching a peak current density of ~65 μA/μm at V_{DS} = 4 V with an I_{on}/I_{off} of > 10^6. This device exhibits good performance with the best current density for an atomically thin (here 2L) $MoSe_2$-based FET reported to date without degradation of the I_{on}/I_{off} ratio.[19,31,33,34,40] Comparable performance was achieved in 2L $MoSe_2$ by Li et al.,[19] although a quantitative comparison is difficult because the channel width was not well defined. The output characteristic of the same device is shown in Figure 4c, where V_{GS} varies from 10 to 60 V with minimal hysteresis. The improved contact resistance and reduced Schottky barrier result in ohmic behavior of the L = 500 nm channel at large positive gate bias. Next, we show that the improved current density in 2L *versus* 1L $MoSe_2$ devices correlates well with reduction in contact resistance.

2.5. $MoSe_2$ Contact Resistance. We use the transfer length method (TLM) and *Y*-function technique to extract the R_C of our AlO_x-capped 1L and 2L $MoSe_2$ FETs, before and after N_2 annealing. For the TLM measurements, we have included short channels of ~100 nm for accurate estimation of R_C.[5] Figure 5a shows the extraction of R_C from the TLM measurement for 1L $MoSe_2$ FETs, where symbols represent experimental data and lines represent the linear fit. The carrier density is evaluated from the linear charge dependence on gate overdrive voltage given by $n \approx C_{ox}(V_{GS} - V_T)/q$ where $C_{ox} \approx$ 38.4 nF/cm^2 is the oxide capacitance for the 90 nm SiO_2, q is the elementary charge, V_{GS} is the gate voltage, and V_T is the threshold voltage determined by the linear extrapolation method for each channel length.

Decent linear fits are obtained for the measured total resistance (normalized by width) R_{TOT} *versus* channel length L for our AlO_x-capped $MoSe_2$ before and after N_2 annealing, signifying relatively uniform properties in the TLM array. The intercept of the linear fit yields $2R_C$, and the slope yields the sheet resistance (R_{sh}). We extract $R_C = 8 \pm 2$ MΩ·μm at 300 K for $n \approx 3.3 \times 10^{12}$ cm^{-2} (with the uncertainty reflecting 96% confidence intervals) for AlO_x-doped 1L $MoSe_2$ (blue). Importantly, R_C is reduced to 1.2 ± 0.4 MΩ·μm at 300 K for $n \approx 5.5 \times 10^{12}$ cm^{-2} with a confidence interval of 98% after N_2 annealing treatment (red). The value of R_{sh} is ~42 MΩ/□ for AlO_x-capped 1L $MoSe_2$, and it decreases to ~14MΩ/□ after N_2 annealing. This is the first characterization of contact resistance in 1L $MoSe_2$, and at this point, a substantial improvement in R_C is needed to meet the requirements for practical applications. It appears that annealing in inert ambient (*e.g.*, N_2) after AlO_x capping is an important step in the reduction of R_C in 1L 2D semiconductors; a similar observation was reported in AlO_x-doped MoS_2 devices.[14]

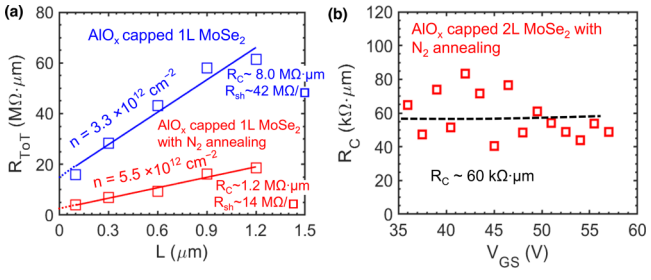


Figure 5. $MoSe_2$ contact resistance. (a) R_{TOT} *vs* channel length (L) for extraction of R_C and R_{sh} before (blue) and after (red) N_2 annealing for AlO_x-capped 1L $MoSe_2$. A significant decrease in R_C and R_{sh} is observed with N_2 annealing at 200 °C for 40 min; symbols are experimental data, and lines are linear fits to the experimental data. (b) R_C *vs* V_{GS} from the *Y*-function method for the 500 nm-long 2L $MoSe_2$ FET. From the strong accumulation regime, we extract an R_C of ~60 kΩ·μm for 2L $MoSe_2$ at V_{DS} = 1 V and a V_{GS} of > 35 V.

For the 2L $MoSe_2$ devices, no TLM arrays were available, and we have therefore used the *Y*-function method[58,59] to evaluate their R_C. Details about *Y*-function fitting are given in Section S3. The *Y*-function extraction for the AlO_x-capped 2L $MoSe_2$ FET after N_2 annealing (L = 500 nm and W = 1.5 μm) shows a V_T of ~18 V (forward sweep) and a μ_0 of ~3 cm^2 V^{-1} s^{-1} (Figure S2). Figure 5b displays R_C extraction using the *Y*-function method at V_{DS} = 1 V. The dashed (black) line represents an averaged R_C value of ~60 kΩ·μm for a V_{GS} of > 35 V. It is noted that the R_C calculated from the *Y*-function[18,58] is an upper bound, and the true R_C could be lower. Our results show that 2L $MoSe_2$ devices achieve ~20× better contact resistance compared with 1L, highlighting the need to optimize the layer number in 1L to FL 2D semiconductor devices.

Before concluding, we note that annealing at 350 °C in inert ambient was performed to test the stability of $MoSe_2$ devices to the back end of the line processing temperatures. 1L devices improved upon annealing (Section S5), whereas 2L devices could not be tested because of the limited number of devices (which underwent electrical breakdown during measurements before this final annealing step). These results suggest that although selenides are less stable in air compared with sulfides, proper encapsulation can provide sufficient protection.

3. CONCLUSIONS

In summary, we report the first study of CVD-grown 1L *versus* 2L $MoSe_2$-based FETs with AlO_x doping. The Raman spectra and mapping depict the individual 1L and 2L devices. A stable electron doping effect was observed for AlO_x-capped 2L devices after N_2 annealing treatment, and an improved current density of ~65 μA/μm and a good I_{on}/I_{off} of > 10^6 with minimal hysteresis were achieved. The 2L $MoSe_2$ devices show ~30× better current density and ~20× lower contact resistance compared with 1L devices. These results also indicate that a two-step process (*i.e.*, AlO_x capping with N_2 annealing) is very promising for the passivation and electron doping of CVD-grown 2L $MoSe_2$ FETs. We conclude that future work in this field should also focus on growing 2L (or otherwise atomically thin FL) $MoSe_2$ and not exclusively 1L for high-performance 2D electronics applications.

4. METHODS

4.1. $MoSe_2$ FET Fabrication. $MoSe_2$ was deposited on 90 nm of thermally grown SiO_2 on Si (p^{++}) substrates (<5 mΩ·cm) using the chemical vapor deposition (CVD) process (Section S1). Electron

https://dx.doi.org/10.1021/acsami.0c09541
ACS Appl. Mater. Interfaces 2020, 12, 36355−36361

beam lithography (EBL) is used to define electrodes, channel area, and probe pads (100 μm × 100 μm) in three separate steps. Au metal electrodes of 50 nm were deposited by e-beam evaporation under high vacuum (~5.8 × 10^{-8} Torr) conditions without any adhesion layer to achieve a clean contact interface. We used O_2 plasma reactive ion etching (pressure = 20 mTorr and an O_2 flow of 20 sccm) for 30 s to form well-defined channels. Furthermore, the contact pads of Ti (15 nm)/Au (50 nm) are deposited by the e-beam evaporation method under a vacuum condition of ~9 × 10^{-7} Torr, followed by lift-off in acetone and IPA cleaning.

4.2. AlO_x Capping and Annealing. Before AlO_x capping, a seed layer of Al metal of thickness ~1.5 nm (a deposition rate of ~0.5 Å/s) was deposited on the $MoSe_2$ devices by e-beam evaporation. The Al seed layer oxidizes upon exposure to air and serves as a nucleation layer for AlO_x. Next, annealing was performed in a forming gas (FG) atmosphere at 250 °C for 30 min. AlO_x (20 nm) was deposited by ALD using trimethylaluminum (TMA) and water (H_2O) as precursors at 150 °C. Before the growth in ALD, we ran 10 nm Al_2O_3 deposition for chamber passivation and ran six washing cycles of TMA. AlO_x covers the whole transistor structure, both the contact region and the channel regions, as shown schematically in Figure 1b. After AlO_x deposition, annealing is performed in a N_2 atmosphere at 200 °C for 40 min to further improve the device characteristics.

4.3. Characterization. The $MoSe_2$ sample topography was first characterized using optical microscopy (Zeiss Axiotron). Raman and PL spectroscopy was carried out using a Horiba LabRam Revolution HR instrument with a 532 nm laser, 1800 1/mm grating, and objective of a 50× long working distance, while a Si peak position at 520 cm^{-1} was used as the standard peak reference. Raman *mapping* was performed with a WITec alpha300 R instrument using 532 nm laser, 1800 g/mm grating, 50x objective lens, and WITec Suite FIVE software for analysis. Raman and PL spectra were employed to characterize the thickness, uniformity, and the material quality of the $MoSe_2$ samples. All the electrical characterizations were carried out with a Keysight B1500 semiconductor parameter analyzer at room temperature in air.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.0c09541.

> CVD growth of $MoSe_2$; effect of AlO_x capping and N_2 annealing on the 1L $MoSe_2$ FET; *Y* function fitting of the AlO_x-capped 2L $MoSe_2$ FET with N_2 annealing; forming gas annealing effect on $MoSe_2$ electrical characteristics; and high temperature annealing effect on $MoSe_2$ electrical characteristics (PDF)

■ AUTHOR INFORMATION

Corresponding Author

Eilam Yalon − *Viterbi Department of Electrical Engineering, Technion-Israel Institute of Technology, Haifa 32000, Israel;* orcid.org/0000-0001-7965-459X; Email: eilamy@technion.ac.il

Authors

Divya Somvanshi − *Viterbi Department of Electrical Engineering, Technion-Israel Institute of Technology, Haifa 32000, Israel*

Emanuel Ber − *Viterbi Department of Electrical Engineering, Technion-Israel Institute of Technology, Haifa 32000, Israel*

Connor S. Bailey − *Department of Electrical Engineering, Stanford University, Stanford, California 94305, United States*

Eric Pop − *Department of Electrical Engineering, Department of Materials Science & Engineering, and Precourt Institute for Energy, Stanford University, Stanford, California 94305, United States;* orcid.org/0000-0003-0436-8534

Complete contact information is available at: https://pubs.acs.org/10.1021/acsami.0c09541

Author Contributions

⊥D.S. and E.B. contributed equally.

Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

Fabrication was carried out at the Technion Micro−Nano Fabrication & Printing Unit (MNF&PU) with partial support from the Russell Berrie Nanotechnology Institute (RBNI). We thank A. Goldner for technical support with EBL, G. Frey and M. Beregovsky for assistance with ALD, and E. Koren and S. Katznelson for providing the Raman mapping setup. D.S. would like to thank the Department of Science and Technology (DST), India, for the INSPIRE faculty award (DST/INSPIRE/04/2017/000147) and for the permission to carry out postdoctoral research work at Technion-IIT Haifa. E.Y. is a Northern Californian Career Development Chair Fellow. C.S.B. and E.P. acknowledge funding from the Stanford System X Alliance and from ASCENT, one of the six centers in JUMP, a Semiconductor Research Corporation (SRC) program sponsored by DARPA.

■ REFERENCES

(1) Chhowalla, M.; Jena, D.; Zhang, H. Two-Dimensional Semiconductors for Transistors. *Nat. Rev. Mater.* **2016**, *1*, 16052.

(2) Jariwala, D.; Sangwan, V. K.; Lauhon, L. J.; Marks, T. J.; Hersam, M. C. Emerging Device Applications for Semiconducting Two-Dimensional Transition Metal Dichalcogenides. *ACS Nano* **2014**, *8*, 1102−1120.

(3) Butler, S. Z.; Hollen, S. M.; Cao, L.; Cui, Y.; Gupta, J. A.; Gutiérrez, H. R.; Heinz, T. F.; Hong, S. S.; Huang, J.; Ismach, A. F.; Johnston-Halperin, E.; Kuno, M.; Plashnitsa, V. V.; Robinson, R. D.; Ruoff, R. S.; Salahuddin, S.; Shan, J.; Shi, L.; Spencer, M. G.; Terrones, M.; Windl, W.; Goldberger, J. E. Progress, Challenges, and Opportunities in Two-Dimensional Materials Beyond Graphene. *ACS Nano* **2013**, *7*, 2898−2926.

(4) Kappera, R.; Voiry, D.; Yalcin, S. E.; Branch, B.; Gupta, G.; Mohite, A. D.; Chhowalla, M. Phase-Engineered Low-Resistance Contacts for Ultrathin MoS_2 Transistors. *Nat. Mater.* **2014**, *13*, 1128−1134.

(5) English, C. D.; Shine, G.; Dorgan, V. E.; Saraswat, K. C.; Pop, E. Improved Contacts to MoS_2 Transistors by Ultra-High Vacuum Metal Deposition. *Nano Lett.* **2016**, *16*, 3824−3830.

(6) Wang, Y.; Kim, J. C.; Wu, R. J.; Martinez, J.; Song, X.; Yang, J.; Zhao, F.; Mkhoyan, A.; Jeong, H. Y.; Chhowalla, M. Van der Waals Contacts between Three-Dimensional Metals and Two-Dimensional Semiconductors. *Nature* **2019**, *568*, 70−74.

(7) Smithe, K. K. H.; English, C. D.; Suryavanshi, S. V.; Pop, E. Intrinsic Electrical Transport and Performance Projections of Synthetic Monolayer MoS_2 Devices. *2D Mater.* **2016**, *4*, 011009.

(8) Schulman, D. S.; Arnold, A. J.; Das, S. Contact Engineering for 2D Materials and Devices. *Chem. Soc. Rev.* **2018**, *47*, 3037−3058.

(9) Allain, A.; Kang, J.; Banerjee, K.; Kis, A. Electrical Contacts to Two-Dimensional Semiconductors. *Nat. Mater.* **2015**, *14*, 1195−1205.

(10) Szabó, Á.; Jain, A.; Parzefall, M.; Novotny, L.; Luisier, M. Electron Transport through Metal/MoS_2 Interfaces: Edge- or Area-Dependent Process? *Nano Lett.* **2019**, *19*, 3641−3647.

(11) Jain, A.; Szabó, Á.; Parzefall, M.; Bonvin, E.; Taniguchi, T.; Watanabe, K.; Bharadwaj, P.; Luisier, M.; Novotny, L. One-

Dimensional Edge Contacts to a Monolayer Semiconductor. *Nano Lett.* **2019**, *19*, 6914−6923.
(12) Passi, V.; Gahoi, A.; Marin, E. G.; Cusati, T.; Fortunelli, A.; Iannaccone, G.; Fiori, G.; Lemme, M. C. Ultralow Specific Contact Resistivity in Metal−Graphene Junctions via Contact Engineering. *Adv. Mater. Interfaces* **2019**, *6*, 1801285.
(13) Rai, A.; Valsaraj, A.; Movva, H. C. P.; Roy, A.; Ghosh, R.; Sonde, S.; Kang, S.; Chang, J.; Trivedi, T.; Dey, R.; Guchhait, S.; Larentis, S.; Register, L. F.; Tutuc, E.; Banerjee, S. K. Air Stable Doping and Intrinsic Mobility Enhancement in Monolayer Molybdenum Disulfide by Amorphous Titanium Suboxide Encapsulation. *Nano Lett.* **2015**, *15*, 4329−4336.
(14) McClellan, C. J.; Yalon, E.; Smithe, K. K. H.; Suryavanshi, S. V.; Pop, E. In *Effective n-type doping of monolayer MoS_2 by AlO_x. 75th Annual Device Research Conference (DRC), 25−28 June 2017*, 2017; pp 1−2.
(15) Moore, G. E. Cramming More Components Onto Integrated Circuits. *Proc. IEEE* **1998**, *86*, 82−85.
(16) Thompson, S. E.; Parthasarathy, S. Moore's law: The Future of Si Microelectronics. *Mater. Today* **2006**, *9*, 20−25.
(17) Huyghebaert, C.; Schram, T.; Smets, Q.; Agarwal, T. K.; Verreck, D.; Brems, S.; Phommahaxay, A.; Chiappe, D.; Kazzi, S. E.; Rosa, C. L. d. l.; Arutchelvan, G.; Cott, D.; Ludwig, J.; Gaur, A.; Sutar, S.; Leonhardt, A.; Marinov, D.; Lin, D.; Caymax, M.; Asselberghs, I.; Pourtois, G.; Radu, I. P. In 2D Materials: Roadmap to CMOS Integration, *IEEE International Electron Devices Meeting (IEDM), 1−5 Dec 2018*, 2018; pp 22.1.1−22.1.4.
(18) Smithe, K. K. H.; Suryavanshi, S. V.; Muñoz Rojo, M.; Tedjarati, A. D.; Pop, E. Low Variability in Synthetic Monolayer MoS_2 Devices. *ACS Nano* **2017**, *11*, 8456−8463.
(19) Li, Y.; Zhang, K.; Wang, F.; Feng, Y.; Li, Y.; Han, Y.; Tang, D.; Zhang, B. Scalable Synthesis of Highly Crystalline $MoSe_2$ and Its Ambipolar Behavior. *ACS Appl. Mater. Interfaces* **2017**, *9*, 36009−36016.
(20) Lee, H.; Deshmukh, S.; Wen, J.; Costa, V. Z.; Schuder, J. S.; Sanchez, M.; Ichimura, A. S.; Pop, E.; Wang, B.; Newaz, A. K. M. Layer-Dependent Interfacial Transport and Optoelectrical Properties of MoS_2 on Ultraflat Metals. *ACS Appl. Mater. Interfaces* **2019**, *11*, 31543−31550.
(21) Zhong, H.; Quhe, R.; Wang, Y.; Ni, Z.; Ye, M.; Song, Z.; Pan, Y.; Yang, J.; Yang, L.; Lei, M.; Shi, J.; Lu, J. Interfacial Properties of Monolayer and Bilayer MoS_2 Contacts with Metals: Beyond the Energy Band Calculations. *Sci. Rep.* **2016**, *6*, 21786.
(22) Li, H.; Yin, Z.; He, Q.; Li, H.; Huang, X.; Lu, G.; Fam, D. W. H.; Tok, A. I. Y.; Zhang, Q.; Zhang, H. Fabrication of Single- and Multilayer MoS_2 Film-Based Field-Effect Transistors for Sensing NO at Room Temperature. *Small* **2012**, *8*, 63−67.
(23) Liu, Y.; Guo, J.; Zhu, E.; Liao, L.; Lee, S.-J.; Ding, M.; Shakir, I.; Gambin, V.; Huang, Y.; Duan, X. Approaching the Schottky−Mott Limit in Van der Waals Metal−Semiconductor Junctions. *Nature* **2018**, *557*, 696−700.
(24) Tongay, S.; Zhou, J.; Ataca, C.; Lo, K.; Matthews, T. S.; Li, J.; Grossman, J. C.; Wu, J. Thermally Driven Crossover from Indirect toward Direct Bandgap in 2D Semiconductors: $MoSe_2$ versus MoS_2. *Nano Lett.* **2012**, *12*, 5576−5580.
(25) Zhang, Y.; Chang, T.-R.; Zhou, B.; Cui, Y.-T.; Yan, H.; Liu, Z.; Schmitt, F.; Lee, J.; Moore, R.; Chen, Y.; Lin, H.; Jeng, H.-T.; Mo, S.-K.; Hussain, Z.; Bansil, A.; Shen, Z.-X. Direct Observation of the Transition From Indirect to Direct Bandgap in Atomically Thin Epitaxial $MoSe_2$. *Nat. Nanotechnol.* **2014**, *9*, 111−115.
(26) Kumar, A.; Ahluwalia, P. K. Electronic Structure of Transition Metal Dichalcogenides Monolayers 1H-MX_2 (M = Mo, W; X = S, Se, Te) From Ab-initio Theory: New Direct Band Gap Semiconductors. *Eur. Phys. J. B* **2012**, *85*, 186.
(27) Zhang, Q.; Chen, Y.; Zhang, C.; Pan, C.-R.; Chou, M.-Y.; Zeng, C.; Shih, C.-K. Bandgap Renormalization and Work Function Tuning in $MoSe_2$/hBN/Ru(0001) Heterostructures. *Nat. Commun.* **2016**, *7*, 13843.
(28) Ugeda, M. M.; Bradley, A. J.; Shi, S.-F.; da Jornada, F. H.; Zhang, Y.; Qiu, D. Y.; Ruan, W.; Mo, S.-K.; Hussain, Z.; Shen, Z.-X.; Wang, F.; Louie, S. G.; Crommie, M. F. Giant Bandgap Renormalization and Excitonic Effects in a Monolayer Transition Metal Dichalcogenide Semiconductor. *Nat. Mater.* **2014**, *13*, 1091−1095.
(29) Gusakova, J.; Wang, X.; Shiau, L. L.; Krivosheeva, A.; Shaposhnikov, V.; Borisenko, V.; Gusakov, V.; Tay, B. K. Electronic Properties of Bulk and Monolayer TMDs: Theoretical Study Within DFT Framework (GVJ-2e Method). *Phys. Status Solidi A* **2017**, *214*, 1700218.
(30) Chamlagain, B.; Li, Q.; Ghimire, N. J.; Chuang, H.-J.; Perera, M. M.; Tu, H.; Xu, Y.; Pan, M.; Xaio, D.; Yan, J.; Mandrus, D.; Zhou, Z. Mobility Improvement and Temperature Dependence in $MoSe_2$ Field-Effect Transistors on Parylene-C Substrate. *ACS Nano* **2014**, *8*, 5079−5088.
(31) Lee, H. A.; Kim, S. Y.; Kim, J.; Choi, W. Effect of Al_2O_3 encapsulation on multilayer $MoSe_2$ thin-film transistors. *J. Phys. D: Appl. Phys.* **2017**, *50*, 094001.
(32) Hong, S.; Im, H.; Hong, Y. K.; Liu, N.; Kim, S.; Park, J. H. n-Type Doping Effect of CVD-Grown Multilayer $MoSe_2$ Thin Film Transistors by Two-Step Functionalization. *Adv. Electron. Mater.* **2018**, *4*, 1800308.
(33) Pradhan, N. R.; Rhodes, D.; Xin, Y.; Memaran, S.; Bhaskaran, L.; Siddiq, M.; Hill, S.; Ajayan, P. M.; Balicas, L. Ambipolar Molybdenum Diselenide Field-Effect Transistors: Field-Effect and Hall Mobilities. *ACS Nano* **2014**, *8*, 7923−7929.
(34) http://2d.stanford.edu/2D_Trends, 2020.
(35) Jeon, J.; Jang, S. K.; Jeon, S. M.; Yoo, G.; Jang, Y. H.; Park, J.-H.; Lee, S. Layer-Controlled CVD Growth of Large-Area Two-Dimensional MoS_2 films. *Nanoscale* **2015**, *7*, 1688−1695.
(36) Lu, X.; Utama, M. I. B.; Lin, J.; Gong, X.; Zhang, J.; Zhao, Y.; Pantelides, S. T.; Wang, J.; Dong, Z.; Liu, Z.; Zhou, W.; Xiong, Q. Large-Area Synthesis of Monolayer and Few-Layer $MoSe_2$ Films on SiO_2 Substrates. *Nano Lett.* **2014**, *14*, 2419−2425.
(37) Liu, B.; Fathi, M.; Chen, L.; Abbas, A.; Ma, Y.; Zhou, C. Chemical Vapor Deposition Growth of Monolayer WSe_2 with Tunable Device Characteristics and Growth Mechanism Study. *ACS Nano* **2015**, *9*, 6119−6127.
(38) Ortiz, D. N.; Ramos, I.; Pinto, N. J.; Zhao, M.-Q.; Kumar, V.; Johnson, A. T. C. Ambipolar Transport in CVD grown $MoSe_2$ Monolayer Using an Ionic Liquid Gel Gate Dielectric. *AIP Adv.* **2018**, *8*, 035014.
(39) Larentis, S.; Fallahazad, B.; Tutuc, E. Field-Effect Transistors and Intrinsic Mobility in Ultra-Thin $MoSe_2$ Layers. *Appl. Phys. Lett.* **2012**, *101*, 223104.
(40) Meng, Y.; Ling, C.; Xin, R.; Wang, P.; Song, Y.; Bu, H.; Gao, S.; Wang, X.; Song, F.; Wang, J.; Wang, X.; Wang, B.; Wang, G. Repairing Atomic Vacancies in Single-Layer $MoSe_2$ Field-Effect Transistor and its Defect Dynamics. *npj Quantum Mater.* **2017**, *2*, 16.
(41) Leonhardt, A.; Chiappe, D.; Afanas'ev, V. V.; El Kazzi, S.; Shlyakhov, I.; Conard, T.; Franquet, A.; Huyghebaert, C.; de Gendt, S. Material-Selective Doping of 2D TMDC through Al_xO_y Encapsulation. *ACS Appl. Mater. Interfaces* **2019**, *11*, 42697−42707.
(42) Yang, M.; Cheng, X.; Li, Y.; Ren, Y.; Liu, M.; Qi, Z. Anharmonicity of monolayer MoS_2, $MoSe_2$, and WSe_2: A Raman Study under High Pressure and Elevated Temperature. *Appl. Phys. Lett.* **2017**, *110*, 093108.
(43) Tonndorf, P.; Schmidt, R.; Böttger, P.; Zhang, X.; Börner, J.; Liebig, A.; Albrecht, M.; Kloc, C.; Gordan, O.; Zahn, D. R. T.; Michaelis de Vasconcellos, S.; Bratschitsch, R. Photoluminescence Emission and Raman Response of Monolayer MoS_2, $MoSe_2$, and WSe_2. *Opt. Express* **2013**, *21*, 4908−4916.
(44) Xia, J.; Huang, X.; Liu, L.-Z.; Wang, M.; Wang, L.; Huang, B.; Zhu, D.-D.; Li, J.-J.; Gu, C.-Z.; Meng, X.-M. CVD Synthesis of Large-Area, Highly Crystalline $MoSe_2$ Atomic Layers on Diverse Substrates and Application to Photodetectors. *Nanoscale* **2014**, *6*, 8949−8955.
(45) Mutlu, Z.; Wickramaratne, D.; Bay, H. H.; Favors, Z. J.; Ozkan, M.; Lake, R.; Ozkan, C. S. Synthesis, Characterization, and Electronic

Structure of Few-Layer $MoSe_2$ Granular Films. *Phys. Status Solidi A* **2014**, *211*, 2671−2676.
(46) Ataca, C.; Topsakal, M.; Aktürk, E.; Ciraci, S. A Comparative Study of Lattice Dynamics of Three- and Two-Dimensional MoS_2. *J. Phys. Chem. C* **2011**, *115*, 16354−16361.
(47) Molina-Sánchez, A.; Wirtz, L. Phonons in Single-Layer and Few-Layer MoS_2 and WS_2. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2011**, *84*, 155413.
(48) Chakraborty, B.; Bera, A.; Muthu, D. V. S.; Bhowmick, S.; Waghmare, U. V.; Sood, A. K. Symmetry-Dependent Phonon Renormalization in Monolayer MoS_2 Transistor. *Phys. Rev. B: Condens. Matter Mater. Phys.* **2012**, *85*, 161403.
(49) Smithe, K. K. H.; Krayev, A. V.; Bailey, C. S.; Lee, H. R.; Yalon, E.; Aslan, Ö. B.; Muñoz Rojo, M.; Krylyuk, S.; Taheri, P.; Davydov, A. V.; Heinz, T. F.; Pop, E. Nanoscale Heterogeneities in Monolayer $MoSe_2$ Revealed by Correlated Scanning Probe Microscopy and Tip-Enhanced Raman Spectroscopy. *ACS Appl. Nano Mater.* **2018**, *1*, 572−579.
(50) Zhang, X.; Sun, D.; Li, Y.; Lee, G.-H.; Cui, X.; Chenet, D.; You, Y.; Heinz, T. F.; Hone, J. C. Measurement of Lateral and Interfacial Thermal Conductivity of Single- and Bilayer MoS_2 and $MoSe_2$ using Refined Optothermal Raman Technique. *ACS Appl. Mater. Interfaces* **2015**, *7*, 25923−25929.
(51) Song, J.-G.; Kim, S. J.; Woo, W. J.; Kim, Y.; Oh, I.-K.; Ryu, G. H.; Lee, Z.; Lim, J. H.; Park, J.; Kim, H. Effect of Al_2O_3 Deposition on Performance of Top-Gated Monolayer MoS_2-Based Field Effect Transistor. *ACS Appl. Mater. Interfaces* **2016**, *8*, 28130−28135.
(52) Somvanshi, D.; Kallatt, S.; Venkatesh, C.; Nair, S.; Gupta, G.; Anthony, J. K.; Karmakar, D.; Majumdar, K. Nature of Carrier Injection in Metal/2D-Semiconductor Interface and its Implications for the Limits of Contact Resistance. *Phys. Rev. B* **2017**, *96*, 205423.
(53) Das, S.; Chen, H.-Y.; Penumatcha, A. V.; Appenzeller, J. High Performance Multilayer MoS_2 Transistors with Scandium Contacts. *Nano Lett.* **2013**, *13*, 100−105.
(54) Liu, W.; Kang, J.; Sarkar, D.; Khatami, Y.; Jena, D.; Banerjee, K. Role of Metal Contacts in Designing High-Performance Monolayer n-Type WSe_2 Field Effect Transistors. *Nano Lett.* **2013**, *13*, 1983−1990.
(55) Sze, S. M.; Ng, K. K. *Physics of Semiconductor Devices*, 3rd ed.; John Wiley & Sons: Hoboken, NJ, 2007.
(56) Chuang, H.-J.; Chamlagain, B.; Koehler, M.; Perera, M. M.; Yan, J.; Mandrus, D.; Tománek, D.; Zhou, Z. Low-Resistance 2D/2D Ohmic Contacts: A Universal Approach to High-Performance WSe_2, MoS_2, and $MoSe_2$ Transistors. *Nano Lett.* **2016**, *16*, 1896−1902.
(57) Zhang, Q.; Zhang, S.; Sperling, B. A.; Nguyen, N. V. Band Offset and Electron Affinity of Monolayer $MoSe_2$ by Internal Photoemission. *J. Electron. Mater.* **2019**, *48*, 6446−6450.
(58) Chang, H.-Y.; Zhu, W.; Akinwande, D. On the Mobility and Contact Resistance Evaluation for Transistors based on MoS_2 or Two-dimensional Semiconducting Atomic Crystals. *Appl. Phys. Lett.* **2014**, *104*, 113504.
(59) Ghibaudo, G. New Method for the Extraction of MOSFET Parameters. *Electron. Lett.* **1988**, *24*, 543−545.

NOTE ADDED AFTER ASAP PUBLICATION

Due to production error, the abstract graphic was incorrect in the version published on July 31, 2020. The corrected paper was reposted on August 3, 2020.

https://dx.doi.org/10.1021/acsami.0c09541
ACS Appl. Mater. Interfaces 2020, 12, 36355−36361

Supporting Information

Improved Current Density and Contact Resistance in Bilayer $MoSe_2$ Field Effect Transistors by AlO_x Capping

Divya Somvanshi[1, 2,†], Emanuel Ber[1,†], Connor S. Bailey[3], Eric Pop[3,4,5], and Eilam Yalon[1,*]

[1]*Viterbi Department of Electrical Engineering, Technion-Israel Institute of Technology, Haifa-32000, Israel*
[2]*Department of Electronics and Tele-Communication Engineering, Jadavpur University, Kolkata-700032, India*
[3]*Department of Electrical Engineering, Stanford University, Stanford, CA 94305, USA*
[4]*Department of Materials Science & Engineering, Stanford University, Stanford, CA 94305, USA*
[5]*Precourt Institute for Energy, Stanford University, Stanford, CA 94305, USA*
[†]*These authors contributed equally*
[*]*E-mail: eilamy@technion.ac.il*

Table of Contents

1. CVD growth of $MoSe_2$

$MoSe_2$ samples were grown via a solid-source CVD method reported previously.[1,2] In short, ~ 100 mg of solid Se pellets was placed into an alumina boat and loaded into the first zone of a two-zone, 2 in. diameter quartz furnace. Another alumina boat containing ~ 0.1 mg of MoO_3 powder was placed 25 cm downstream from the Se source in the second, higher temperature zone of the furnace. The Si/SiO_2 growth substrate was first treated with hexamethyldisilazane (HMDS) and perylene-3, 4, 9, 10-tetracarboxylic acid tetra potassium salt (PTAS) before being placed face down about 5 mm above the MoO_3. After purging with Ar flowing at 1000 sccm for 5 min, the Se zone was heated to 500°C and the main growth zone to 850°C. For the growth phase, a gas flow of 25 sccm

Ar and 5 sccm H_2 was maintained for 30 min, after which the furnace temperature was ramped down under inert Ar flow until cooled to room temperature.

2. Effect of AlO_x capping and N_2 annealing on 1L $MoSe_2$ FET

Figure S1 shows dual sweep log-scale transfer characteristics of bare (black), AlO_x capped (blue), and AlO_x capped after N_2 annealing (red) 1L $MoSe_2$ FET (L= 1.4 µm) at V_{DS} = 1V. We see an increase in I_D from 0.06 nA/µm to 13.63 nA/µm at V_{GS} = 30V for bare and AlO_x capped 1L $MoSe_2$ FET respectively. There is also a significant change in the hysteresis observed for these devices after AlO_x capping which is comparable to 2L $MoSe_2$ devices. These changes are largely attributed to AlO_x passivation effect. After N_2 annealing is performed, another increase in I_D is observed (37.7 nA/µm), but no p-type branch is observed for 1L FETs regardless to capping or annealing processes.

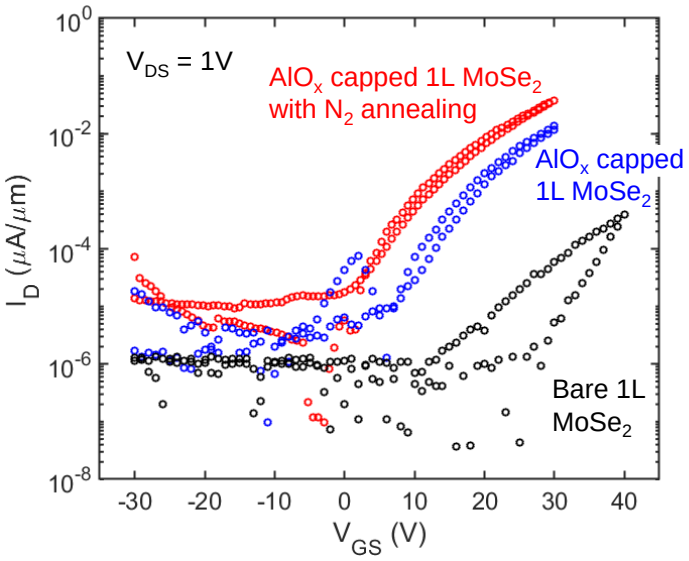


Figure S1. Dual sweep log-scale transfer characteristics of bare, AlO_x capped, and N_2 annealed 1L $MoSe_2$ FET at V_{DS} = 1V, measured in air. An increase in I_D, I_{on}/I_{off} and a decrease in hysteresis is observed after capping with AlO_x and annealing in N_2.

3. Y function fitting of AlO_x capped 2L $MoSe_2$ FET with N_2 annealing

To evaluate the contact resistance of the 2L devices, we used the Y-function method, which is based on the analysis of I_D in the FET linear regime. Figure S2 shows the Y-function fitting extraction of the threshold voltage (V_T), mobility (μ_0) and contact resistance (R_C) of a 500-nm long AlO_x capped 2L $MoSe_2$ FET, after N_2 annealing at V_{DS} = 1 V. Considering that the Schottky-barrier induced contact resistance will result in additional voltage drops, the drain current (I_D) can be expressed as[3]

$$I_D = \left(\frac{\mu_o}{1+\theta_o (V_{GS} - V_T)} \right) C_{ox} \frac{W}{L} (V_{GS} - V_T - 0.5V_{DS})(V_{DS} - I_D R_c) \qquad (1)$$

Where θ_0 is the first-order mobility attenuation coefficient, $C_{ox} \approx 38$ nF cm^{-2} is the capacitance per unit area of 90 nm SiO_2, W and L are the width and length of the channel, V_{GS} and V_{DS} are the gate and drain voltage, and V_T is the threshold voltage obtained by the linear extrapolation method. The Y-function is defined as $I_D / \sqrt{g_m}$, where g_m is the transconductance, which is defined as dI_D/dV_{GS}. The Y-function is written as [4]

$$Y = \frac{I_D}{\sqrt{g_m}} = \frac{\sqrt{\mu_o C_{ox} V_{DS} \frac{W}{L}}}{\sqrt{1 - \mu_o C_{ox} R'_c \frac{W}{L} (V_{GS} - V_T)^2}} (V_{GS} - V_T) \qquad (2)$$

Where R'_c is dR_C/dV_{GS}. By assuming that R_C is not gate dependent in eq.(2) we can extract μ_0 and V_T from the simplified expression given as $Y = (\mu_o C_{ox} V_{DS} W/L)^{0.5} (V_{GS} - V_T)$. From the linear fit in the strong electron accumulation regime, V_T ~ 18 V (forward sweep) and $\mu_0 \sim 3$ cm^{2}V^{-1}s^{-1} are extracted from the x-intercept and the slope, respectively.

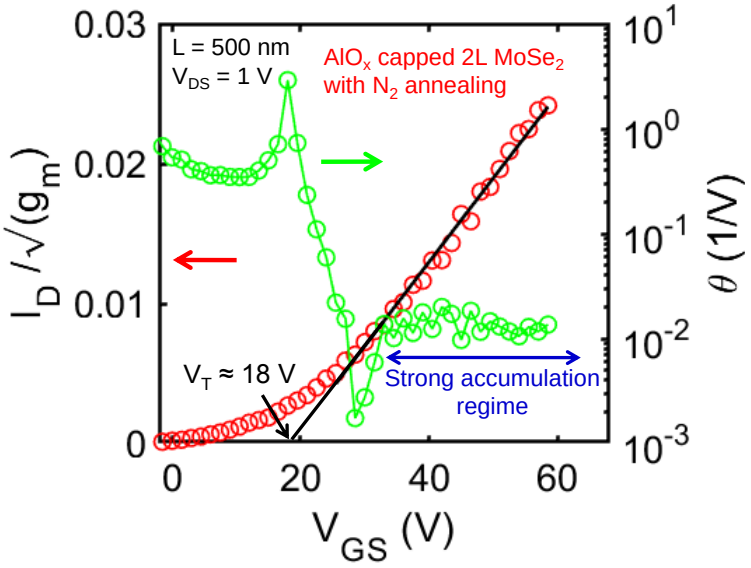


Figure S2. AlO_x capped 2L $MoSe_2$ FET with N_2 annealing. The linear fitting of the forward sweep of Y-function vs. V_{GS} plot (left axis) shows good agreement with the experimental data (symbol). Both V_T ~ 18 V and μ_0 ~ 3 $cm^2V^{-1}s^{-1}$ are extracted from the x-intercept and the slope respectively at V_{DS} = 1 V. From θ vs. V_{GS} characteristics (right axis), the value of R_C ~ 60 kΩ·µm is extracted from the strong accumulation regime.

4. Forming gas annealing effect on $MoSe_2$ electrical characteristics

Annealing in forming gas (FG) was used to reduce fixed oxide charges and interface states.[5] We have performed annealing in FG (95 % N_2 +5% H_2) ambient at 250 ºC for 30 minutes on the AlO_x capped 2L $MoSe_2$ devices after N_2 annealing. Figure S3 compares transfer characteristics of as-prepared AlO_x capped 2L $MoSe_2$ FET with N_2 and FG annealed devices at V_{DS} =1V. A negative shift in V_T ~ -2.8 V is observed with slightly improved I_{on}, hysteresis, and I_{on}/I_{off} ratio. Comparing the change from as-prepared devices this could indicate that annealing in inert gas (N_2) ambient is more effective than FG to increase electron doping in $MoSe_2$ FETs as was observed in MoS_2 FETs.[6] However, this cannot be determined conclusively because this effect could also be a result of the thermal annealing history (just due to the sequenced anneals).

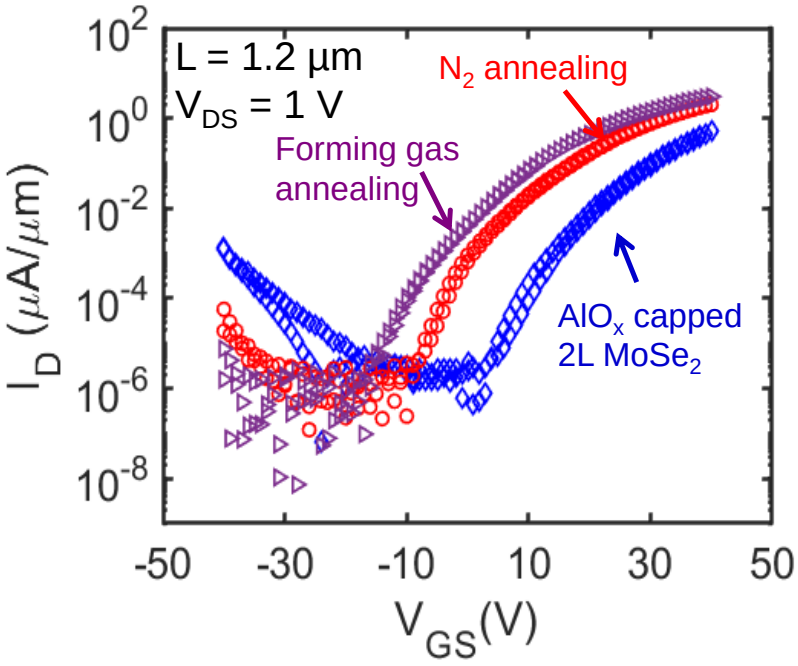


Figure S3. Transfer characteristics of AlO_x capped $MoSe_2$ FETs comparing the as prepared, N_2 annealed (200 ºC for 40 minutes), and FG annealed (250 ºC for 30 minutes) devices. FG annealing took place after N_2 annealing. A negative shift in V_T ~ - 2.8 V, and a small improvement in I_{on} and I_{on}/I_{off} is observed after FG annealing with respect to N_2 annealing.

5. High temperature annealing effect on $MoSe_2$ electrical characteristics

High temperature (350 ºC) annealing was performed in order to verify that the $MoSe_2$ devices retain their performance after thermal treatments that are within the thermal budget of back end of the line (BEOL) processing. We have performed annealing in inert ambient (3 mTorr and flow of 50 sccm Ar) at 350 ºC for 20 minutes on the AlO_x capped $MoSe_2$ devices. Figure S4 compares the transfer characteristics of an AlO_x capped 1L $MoSe_2$ FET before and after high temperature annealing. A negative shift in V_T ~ -3.5 V is observed with improved I_{on}, and I_{on}/I_{off} ratio. The improvement in device characteristics suggest that the device not only remains stable, but also improves throughout exposure to temperatures corresponding to BEOL processing. This improvement can be attributed to enhancement of the electron doping effect as well as evaporation of resist residue.

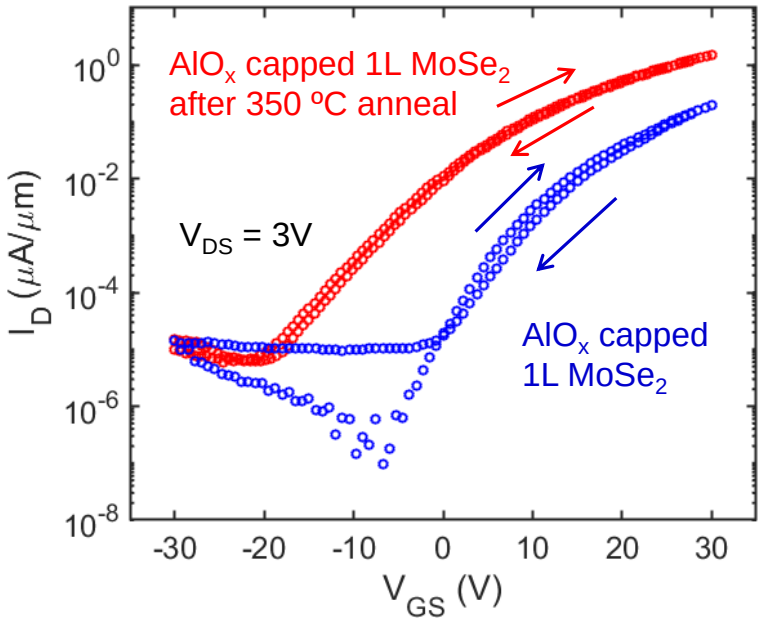


Figure S4. Transfer characteristics of an AlO_x capped $MoSe_2$ FET before and after high temperature (350º C) annealing. The transfer curve shows a negative shift in V_T ~ -3.5 V, and ~10× improvement in I_{on} while I_{off} is preserved.

Supporting Information References:

1. Smithe, K. K. H.; Krayev, A. V.; Bailey, C. S.; Lee, H. R.; Yalon, E.; Aslan, Ö. B.; Muñoz Rojo, M.; Krylyuk, S.; Taheri, P.; Davydov, A. V.; Heinz, T. F.; Pop, E., Nanoscale Heterogeneities in Monolayer $MoSe_2$ Revealed by Correlated Scanning Probe Microscopy and Tip-Enhanced Raman Spectroscopy. *ACS Appl. Nano Mater.* **2018,** *1* (2), 572-579.

2. Chen, J.; Bailey, C. S.; Cui, D.; Wang, Y.; Wang, B.; Shi, H.; Cai, Z.; Pop, E.; Zhou, C.; Cronin, S. B., Stacking Independence and Resonant Interlayer Excitation of Monolayer $WSe_2/MoSe_2$ Heterostructures for Photocatalytic Energy Conversion. *ACS Appl. Nano Mater.* **2020,** *3* (2), 1175-1181.

3. Ghibaudo, G., New Method for the Extraction of MOSFET Parameters. *Electron. Lett.* **1988,** *24* (9), 543-545.

4. Chang, H.-Y.; Zhu, W.; Akinwande, D., On the Mobility and Contact Resistance Evaluation for Transistors Based on MoS_2 or Two-Dimensional Semiconducting Atomic Crystals. *Appl.Phys. Lett.* **2014,** *104* (11), 113504.

5. Mirabelli, G.; Walsh, L. A.; Gity, F.; Bhattacharjee, S.; Cullen, C. P.; Ó Coileáin, C.; Monaghan, S.; McEvoy, N.; Nagle, R.; Hurley, P. K.; Duffy, R., Effects of Annealing Temperature and Ambient on Metal/$PtSe_2$ Contact Alloy Formation. *ACS Omega* **2019,** *4* (17), 17487-17493.

6. McClellan, C. J.; Yalon, E.; Smithe, K. K. H.; Suryavanshi, S. V.; Pop, E. Effective n-Type Doping of Monolayer MoS_2 by AlO_x, 75th Annual Device Research Conference (DRC), 25-28 June 2017; 1-2.