Applied Physics Letters ARTICLE scitation.org/journal/apl

Temperature-dependent thermal resistance of phase change memory

Cite as: Appl. Phys. Lett. **120**, 113501 (2022); doi: 10.1063/5.0081016
Submitted: 6 December 2021 · Accepted: 2 March 2022 ·
Published Online: 14 March 2022

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ABSTRACT

One of the key challenges of phase change memory (PCM) is its high power consumption during the reset operation, when the phase change material (typically $Ge_2Sb_2Te_5$, i.e., GST) heats up to ~900 K or more in order to melt. Here, we study the temperature-dependent behavior of PCM devices by probing the reset power at ambient temperatures from 80 to 400 K. We find that different device structures exhibit contrasting temperature-dependent behavior. The reset power in our confined-type PCM is nearly unchanged with ambient temperature, corresponding to a temperature-dependent thermal resistance, whereas results for mushroom-type PCM from the literature show a linear relation between power and temperature, suggesting a more constant thermal resistance. This discrepancy is ascribed to different temperature distributions and thermal properties of the dominant components of the PCM cell thermal resistance, as shown by electro-thermal modeling. In the confined cell, the thermal boundary resistance of the GST and the thermal conductivity of the bottom electrode dominate the thermal resistance, while for the mushroom cell, the GST thermal conductivity plays a greater role. These findings can help to design more power- and energy-efficient PCM devices by better focusing thermal management efforts on the key components of the device.

Phase change memory (PCM) is a relatively mature non-volatile data storage technology that has already been commercialized as a storage-class memory[1] and is currently a leading candidate for neuromorphic computing.[2–5] PCM is made of chalcogenides, usually $Ge_2Sb_2Te_5$ (GST), which can store data coded by its phase, e.g., amorphous (with high electrical resistivity) and crystalline (low electrical resistivity), as illustrated in Fig. 1(a).[6] Switching between these states is achieved by applying voltage pulses that generate Joule heating. Starting from an amorphous phase, increasing the temperature above the crystallization temperature for sufficient time (usually few tens or hundreds of nanoseconds) will result in the crystalline phase; this process is referred to as set. Heating the PCM above its melting temperature and rapidly quenching it below the crystallization temperature before it can crystallize will amorphize the material; this process is called reset.

By its nature, it can be understood that reset is a power- and energy-hungry process, and many studies have investigated ways to better confine the heat and minimize its dissipation, such as new materials and interfaces,[7–11] device architectures,[12–14] and programming pulse reduction to minimize the heat diffusion time.[15,16] In this context, special attention must be given to the thermal resistance of the PCM device,[17] because it determines its heating efficiency. It is important to understand what the dominant thermal components are, their dependence on materials, interfaces, and device structure, as well as their behavior in a wide range of operating temperature.[18]

This work aims to improve our understanding of PCM thermal resistance by investigating its temperature dependence and the impact on reset power consumption. We show that confined PCM structures exhibit a different thermal behavior compared with mushroom cells. For a constant thermal resistance (R_{th}), a linear relation between reset power (P) and ambient temperature (T_{amb}) is expected: $P \cdot R_{th} = (T_{melt} - T_{amb})$, as shown in Fig. 1(b). Previous studies have shown such behavior in mushroom cells;[13,18] however, we reveal that reset power in confined PCM cells remains nearly unchanged with ambient temperature in the range 80 to 400 K, suggesting that the thermal resistance decreases with (increasing) temperature. As a consequence, the temperature dependence of the thermal conductivity (k_{th}) of certain materials and interfaces (thermal boundary resistance, TBR) cannot be neglected[19–21] and must be considered to understand the total thermal resistance of the device. The experimental results are explained by a finite element electro-thermal model, which includes the temperature-dependent thermal and electrical properties.

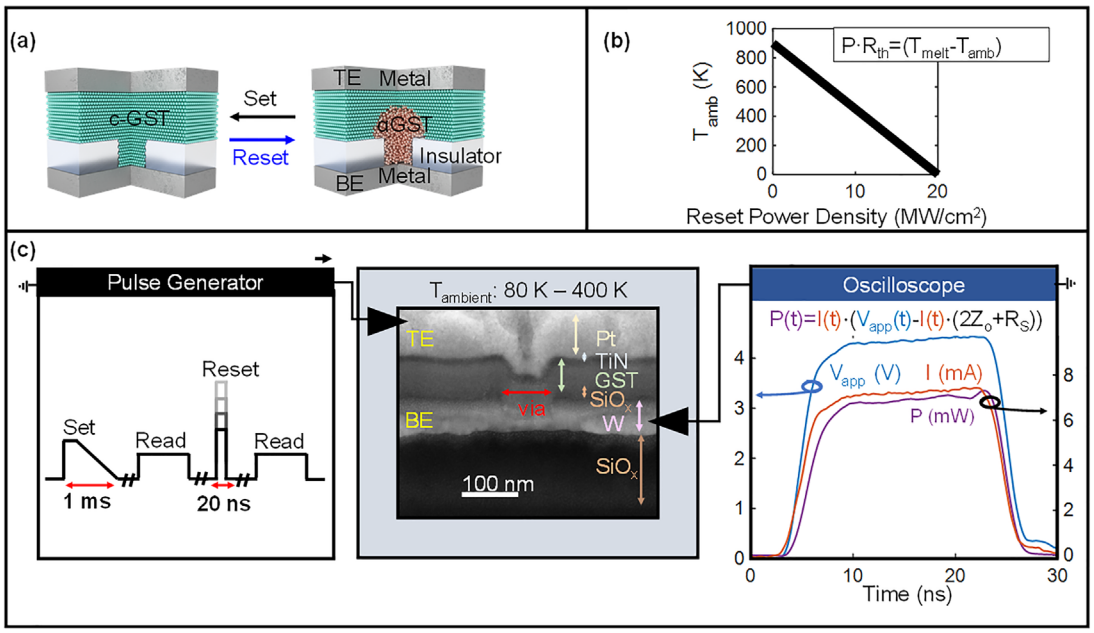

FIG. 1. (a) Schematic of a confined PCM cell. The GST is sandwiched between the top and bottom (TE and BE) metal electrodes, and the active area is surrounded by an insulator to confine the heat generated by electrical pulses. The crystalline GST on the left (green) is switched to the amorphous phase (pink) on the right in a melt-quench process (reset). Reversible switching is achieved by heating to the crystalline temperature (set). (b) A linear relation between ambient temperature and reset power density is expected with constant thermal resistance (R_{th}). For certain materials and interfaces, the R_{th} temperature dependence cannot be neglected and the relation is not linear. (c) Experimental setup used to probe power in our confined PCM cells. The PCM was measured in a cryo-probe-station chamber under varying ambient temperatures from 80 to 400 K. The device was connected in series to a pulse generator (left) and a oscilloscope (right). A cross-sectional SEM (scanning electron microscopy) image of the device is shown in the middle. GST is the active material, TiN/Pt were TE, W was BE, SiO_2 was the insulator, and Si was the substrate (not shown). The TE is connected to a pulse generator on the left, and the programming scheme is illustrated in the pulse generator panel. For each ambient temperature, the initially crystalline PCM was subjected to reset pulses with gradually increased power, followed by a long read pulse (after each reset pulse). The BE was connected to the oscilloscope on the right, allowing us to capture the current (orange) and the applied voltage (blue) to extract the power (purple).

To probe power consumption at varying ambient temperatures, we carried out measurements in vacuum in a Janis Research (Lakeshore Cryotronics) ST-500-UHT micromanipulated probe station with microwave ground-signal (GS) probes. Temperature was controlled by a Lakeshore Model 336 controller. We measured confined PCM devices with 175 nm nominal via diameter. The device was connected in series to a pulse generator with $Z_0 = 50\ \Omega$ load resistance, and a high-speed (8 GHz) scope with $Z_0 = 50\ \Omega$ termination, to probe the current during the pulse. We varied the ambient temperature in the range of 80 to 400 K. The PCM was first set to its lowest resistance, indicating the crystalline hexagonal close-packed (hcp) phase, in the range of ~0.5 to 0.7 kΩ. Reset pulses of 20 ns width, 2.5 ns rise fall times, with gradually increasing voltage amplitudes were applied, and the resistance was read under low (0.2 V) DC bias after each pulse. It is important to note that 20 ns pulse duration was chosen in order to collect data after the device reached thermal steady state, which can be estimated by the thermal time constant. More details about the device thermal time constant at different ambient temperatures can be found in Sec. 4 in the supplementary material and in our previous work on PCM energy limits.[15] Figure 1(c) illustrates the setup, programming scheme, PCM confined structure, and power extraction. More details on the measurement technique and the data analysis can be found in Ref. 15, experimental section.

Our main results are depicted in Fig. 2, showing the change in resistance following reset pulses with the increasing amplitude [vs power in Fig. 2(a) and current in Fig. 2(b)] at varying ambient temperatures. The key finding is that the reset power remains nearly unchanged as the ambient temperature is varied from 80 to 400 K. Recalling that for constant thermal resistance a linear relation is expected between reset power and ambient temperature [Fig. 1(b)], our results indicate that the thermal resistance of our confined cells depends on temperature, and this cannot be neglected. To validate that the same PCM volume was melted at each ambient temperature, we also performed resistance vs ambient temperature measurements of fully amorphous PCM, shown in Fig. 2(b) inset. The graph exhibits almost two order of magnitude change of resistance in the measured temperature range due to the exponential dependence of the electrical conductivity on temperature in the amorphous state, in contrast to that of the crystalline hcp phase.[22] This result suggests that roughly the same PCM volume was melted (and quenched) in the range of 80 to 400 K, because the final resistance following reset pulses carried out at each temperature is similar to the resistance of PCM that was reset at room temperature and then probed at that ambient temperature (varying between 80 and 400 K).

The reset power densities for each measured ambient temperature of our confined PCM, obtained from Fig. 2(a), are summarized in

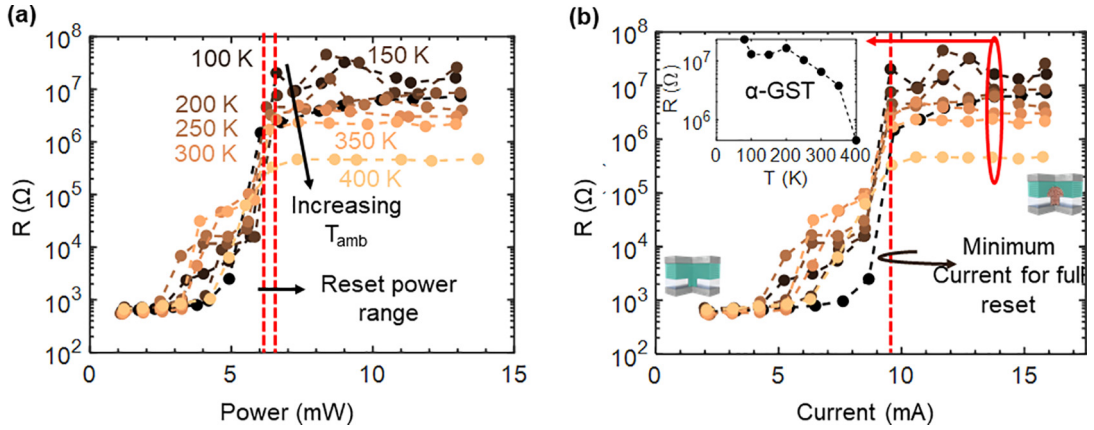

FIG. 2. Read resistance after each reset pulse vs (a) power consumption and (b) current during the pulse at different ambient temperatures. Circles represent the final read resistance after each reset pulse, and the gradual colors represent different ambient temperatures, dark to light color for lowest to the highest temperature, respectively. Each point in the graph represents a measurement that started at a fully crystalline (low resistance) state; power and current are measured during the reset pulse. (a) In red dashed lines, a minimum power window for reset is marked, indicating that reset power remains nearly unchanged. (b) Roughly the same reset current during the pulse is observed for each temperature, marked in a red dashed line. The inset shows resistance (in log scale) vs temperature of fully amorphous PCM. The a-GST resistance increases by more than an order of magnitude as the temperature decreases in the measured range. From this, we can conclude that the difference in final resistance vs temperature is due to the a-GST resistivity rather than its volume; hence, roughly the same PCM volume was melted in the range of 80 to 400 K (marked in a red circle).

Fig. 3 (blue) and compared to results of mushroom cells reported by Kersting *et al.*[23] (orange). The mushroom cells exhibit linear relation between power density and ambient temperature with a constant thermal resistance (the slope) $R_{th} \sim 1\ \mu m^2$ K/mW ($=10^{-5}$ cm^2 K/W), whereas the confined cells show only very minor changes in reset power with (ambient) temperature (within less than 10%). This result points to a temperature-dependent thermal resistance of the confined PCM, as outlined earlier; hence, the importance of the cell structure in considering its thermal behavior stands out. The notable dissimilarity in thermal resistance between confined and mushroom cells can be explained by the difference in heat dissipation of the two structures.

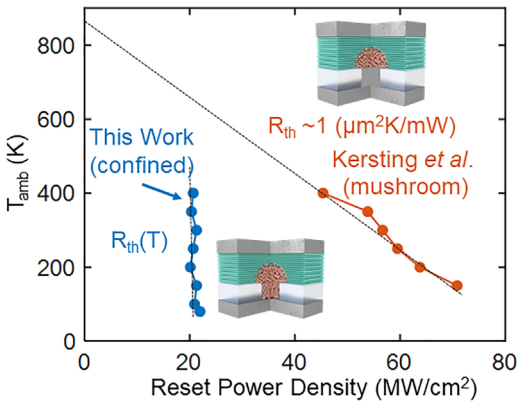

FIG. 3. Ambient temperature vs reset power density. Blue circles represent our work on confined PCM, orange circles represent measurements by Kersting *et al.*[23] for mushroom cells. The mushroom cell exhibits constant R_{th} with linear power-temperature linear relation. For the confined PCM case, the observed R_{th} is strongly temperature-dependent, and reset power consumption remains nearly unchanged with ambient temperature.

The electro-thermal simulations below show that the confined cells are dominated by the thermal boundary resistance (TBR) of the bottom interface, as well as the bottom electrode (BE), whereas the mushroom cell is dominated by the GST itself and the heater, whose temperatures are nearly independent of the ambient temperature at reset conditions. We note that the thermal resistance relates the temperature rise with the applied power, but PCM reset also requires a phase transition from crystalline to amorphous, so the latent heat of fusion should also be considered. In our previous study,[15] we have shown that typical PCM reset energies are larger by several orders of magnitude compared with the adiabatic limit (thermally isolated PCM cell). This lower limit case includes the heating energy to reach the melting temperature of a given PCM volume and the latent heat. The value of the GST latent heat of fusion[24,25] is compared to the reset energy of a perfectly thermally insulated device in Sec. 2 of the supplementary material. The comparison shows that the latent heat portion of the reset energy for a perfectly insulated device is ∼10%. Details about the reset energy model can be found in Ref. 15.

Thermoelectric effects may also play a role in the heating of the PCM.[26–29] To examine the role of Peltier heating, we include experimental results with opposite voltage polarity and to account for both Peltier and Thomson effects we carried out simulations as shown in Sec. 3 of the supplementary material. Note that only the GST itself has a meaningful Seebeck coefficient (S) but its temperature at the reset condition is nearly unchanged with the ambient temperature, because it has to reach the melting temperature. The role of thermoelectric heating therefore does not dominate the observed temperature-dependent thermal behavior of our PCM devices.

To better understand the thermal behavior of PCM devices, we carried out finite element electro-thermal simulations. The simulated temperature maps displayed in Fig. 4 show similar "melted" volume of the PCM ($T > T_M$, where T_M is the melt temperature of the GST) of confined and mushroom cells with varying ambient temperature, and

their minimum reset power (the lowest power needed to melt the critical PCM volume shown). Importantly, the simulations account for temperature-dependent thermal properties of the materials, as detailed in Table S1 in the supplementary material. Briefly, the thermal conductivity of the metal electrodes, hcp-GST, and melt-GST include the electronic thermal conductivity component, which is obtained from the Wiedemann–Franz law (WFL) based on their electrical conductivity and the phonon thermal conductivity component.[30] Across the operation temperature range of the device, these are dominated by the electronic component, which has a linear dependence on temperature when the electrical conductivity is constant (based on WFL). The Pt total thermal conductivity (electrical and phonon) was taken from Ref. 31, W electrical resistivity at 300 K was set to 25 $\mu\Omega$ cm based on Ref. 32 for a thin layer of 40 nm, and the W phonon thermal conductivity of 3 W/m/K was obtained from Ref. 33. For the TiN layer, the electrical conductivity was taken from Ref. 34 and the phonon thermal conductivity of 1 W/m/K was determined by subtracting the electronic component at 300 K from the total thermal conductivity that was reported in Ref. 35. The GST TBR was first determined as a fitting parameter to match one of the measurements, within values in the range reported in the literature,[19,36] and then, the same value was used for all simulations. The electrical conductivity of hcp-GST was measured in our devices, as detailed in supplementary material Sec. 4.

With these temperature-dependent thermal (and electrical) properties, the simulations reproduce the trends obtained experimentally, namely, the confined cells show nearly unchanged reset power with ambient temperature, whereas the mushroom cells show linear relation between reset power and ambient temperature. The simulated temperature maps help to visualize the difference in heat dissipation across the different structures and uncover the origin of the thermal behavior. In both cases, the Si substrate (not shown in the figure) acts as the heat sink; hence, heat flows predominantly toward the bottom, with some heat spreading laterally in the GST, SiO_x, and the BE. In the mushroom cell, the active PCM area is separated from the BE by the heater, so the thermal resistance is dominated by the GST itself and by the heater. During reset, both the GST and the heater are heated to high temperature, close to that of the melt, regardless of the ambient temperature of the thermal sink. This explains the constant thermal resistance of the mushroom cell, which exhibits linear dependence between reset power and ambient temperature. In the confined cell on the other hand, the temperature of the BE in vicinity of the melted GST is highly dependent on the ambient (sink) temperature.

The electro-thermal simulations show that the thermal resistance of the confined cell is dominated by the BE and the TBR of the GST (with its surrounding, namely, the BE and SiO_x). The thermal conductivity of the metallic bottom electrode and the thermal boundary conductance (1/TBR) of the GST increase with temperature, which explains why the thermal resistance of the confined cell decreases with temperature. We also carried out experiments and simulations to test the size scaling trend of our devices, which show that as the confined cell scales up its interfaces becomes less dominant (see supplementary material Sec. 5). These findings can help to design more power-efficient PCM devices. For example, in certain structures (e.g., confined), more focus should be given to the material and thickness of the bottom electrode, whereas in other structures (e.g., mushroom) to the PCM itself.

In summary, we measured temperature-dependent reset power in confined PCM cells in a wide range of ambient temperatures (80 to 400 K) and compared their thermal resistance to that of mushroom cells reported in the literature. Our confined cells show nearly

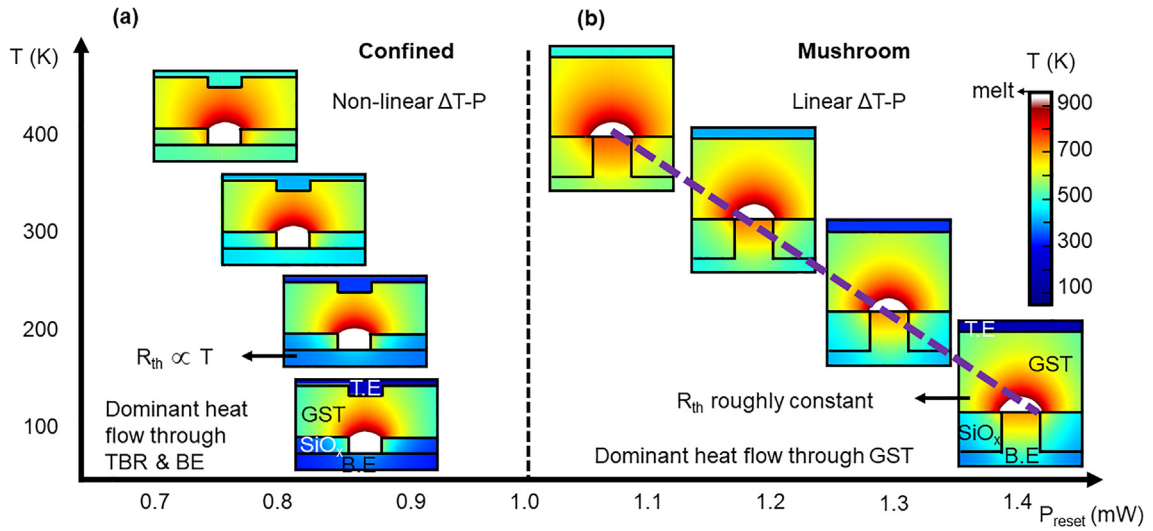

FIG. 4. Simulated temperature maps and reset power under varying ambient temperature. The electro-thermal simulations reproduce the different relation of ambient temperature and power for two different device structures: (a) confined cell and (b) mushroom cell. The white-colored area represents the melted volume and colors present the temperature according to the color-bar shown on the right. Specific (temperature-dependent) thermal properties are identical in both cases and are detailed in Table S1 in supplementary material Sec. 1. In the confined cell (a), the dominant part of the heat flows through the bottom interface (thermal boundary resistance, TBR) and the bottom electrode (BE). The temperatures of the BE and the bottom interface change with the ambient temperature, causing a temperature-dependent thermal resistance. In the mushroom cell (b) much of the heat dissipates through the GST and the heater. Because the temperature of both GST and the heater (at reset conditions) have a very weak dependence on the ambient temperature, the thermal resistance is roughly constant and a linear relation between reset power and ambient temperature is obtained.

unchanged reset power with ambient temperature in the entire measured range, suggesting that their thermal resistance decreases linearly with temperature, whereas mushroom cells show linear dependence of reset power on ambient temperature, as expected for constant thermal resistance (with respect to temperature). We also carried out electro-thermal simulations, including the temperature-dependent electrical and thermal properties of the materials and their interfaces, which capture the trend obtained experimentally and help to explain its origin. The simulations show that the thermal resistance of the confined cells is dominated by their thermal boundary resistance as well as the bottom electrode, whereas the mushroom cell is dominated by the GST itself and the heater. Such findings can help to design more power-efficient PCM devices, by focusing thermal management efforts on the components of the device that dominate its thermal resistance.

See the supplementary material for details on the thermal and electrical properties used in the simulations, transient resistance measurements to extract electrical conductivity of melted GST, and effect of varying vias size.

This work was supported in part by ISF Grant No. 1179/20, by Russel Berrie Nanotechnology Institute (RBNI), and by member companies of the Stanford Non-volatile Memory Technology Research Initiative (NMTRI). Fabrication of the confined PCM cells was performed at the Stanford Nanofabrication Facility (SNF) and Stanford Nano Shared Facilities (SNSF). Fabrication of the transmission lines was carried out at the Technion Micro-Nano Fabrication & Printing Unit (MNF&PU).

AUTHOR DECLARATIONS

Conflict of Interest

The authors declare no conflict of interest.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Supporting Information

Temperature-Dependent Thermal Resistance of Phase Change Memory

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Section 1 – Thermal and Electrical Properties

Table S1 summarizes the thermal and electrical properties of the materials used in the simulations with their respective sources or references. The "comments" tab defines the components of the total thermal conductivity (k_{th}). The electrical contact resistance was determined by an effective thickness t_{eff} = 10 nm of the GST as defined in ref. [1]. The temperature dependence of the GST-SiO_x thermal boundary resistance (TBR) was determined as a fitting parameter, and its room temperature value was taken from ref.[2]; The TBR of GST with other materials were determined as equal to that of GST-SiO_x to simplify the simulation. The thermal conductivity of hcp-GST and the electrodes were evaluated by two contributions of electron thermal conductivity (k_e) and the lattice thermal conductivity (k_{ph}). k_e was evaluated from the electrical conductivity using the Wiedemann–Franz law (WFL), and k_{ph} was extracted from total k_{th} at 300 K with the subtraction of k_e under the assumption of constant k_{ph}. For GST, we used k_{ph} value at high-temperature (near melt) of ~0.1 W/m/K, assuming it is lower than the room-temperature value from literature 0.4 W/m/K,[2] because the melt is disordered like the amorphous phase, so phonons tend to scatter more than the ordered hcp phase. The Seebeck coefficients for the electrodes were assumed to be zero since they are negligible compared to that of the GST semiconductor.[3,4] The hcp-GST Seebeck coefficient was set to 50 µV/K, based on values from the literature of ~20-50 µV/K near the GST melting temperature.[4,5]

A "through" device (without the GST) resistance was measured to evaluate the dependence of the combined electrodes' electrical conductivity (σ) on temperature. No major change was obtained experimentally in the ambient temperature range operation of the device (80 K to 400 K), hence the electrodes' electrical conductivities σ were chosen to be constant, in accordance with literature.[6] For GST- hcp and GST-melt, the electrical conductivity σ was evaluated by a melt resistance measurement, as shown in section 3, Fig. S2a, and the obtained values are in good agreement with previous measurements.[7]

Table S1 – Temperature-dependent thermal properties for electro-thermal simulations						
Material	**k_{th} (W/m/K)**	**Comments**	**TBR (m^2K/W)**	**σ (S/m)**	**S (V/K)**	**Ref.**
GST-hcp	$\sigma \cdot L_0^* \cdot T + 0.1$	$k_e + k_{ph}$	$2 \cdot 10^{-2} \cdot T^{-2}$	$2 \cdot 10^4$	$5 \cdot 10^{-5}$	Fig. S2a, [4,5]
SiO_2	$\ln(T^{0.52}) - 1.6$		$0.1 \cdot 10^{-2} \cdot T^{-2}$	10^{-10}	0	[8]
W	$\sigma \cdot L_0^* \cdot T + 3$	$k_e + k_{ph}$		$4 \cdot 10^6$	0	[6,9]
TiN	$\sigma \cdot L_0^* \cdot T + 1$	$k_e + k_{ph}$		$2.5 \cdot 10^5$	0	[10,11]
Pt	$\sigma \cdot L_0^* \cdot T + 10$	$k_e + k_{ph}$		$1 \cdot 10^6$	0	[12]

*$L_0 = 2.4 \cdot 10^{-8}\ W\Omega/K^2$ (Lorentz number)

Section 2 – Latent heat of fusion

From a thermodynamic perspective, we can estimate the lowest energy required to reset a PCM cell as follows: $E_{min} = C_S \Delta T_M + H \approx 0.9$ aJ/nm^3, where $C_S \approx 1.3$ J·cm^{-3}K^{-1},[2] is the GST specific heat, $\Delta T_M \approx 600^oC$ is the temperature rise for melting, and $H \approx 100$ J·cm^{-3} is the latent heat of melting. [13,14] This is the energy (per unit volume) needed to reset a PCM cell that is perfectly insulated thermally (adiabatically) from its environment. This is also equivalent to an infinite thermal boundary resistance (TBR → ∞) at the PCM interface with the metal electrodes and the dielectric layers surrounding it. In this adiabatic case the latent heat of melting *H* is ~10% of the reset energy, but when comparing it to reset energy with heat loss to the environment, the *H* portion becomes much lower (less than ~1%). Calculated values can be found in ref. [7].

Section 3 – Thermoelectric effects

To examine the impact of Peltier heating, measurements for positive and negative polarity were performed (Fig. S1a). In addition, the device was simulated with and without thermoelectric effects (Peltier and Thomson) as shown in Fig. S1b,c. The key finding is that thermoelectric effects in the simulation are responsible for up to ~15% of the total reset power at 100 K and 400 K ambient temperature. The effects at 100 K and 400 K are roughly the same, because the GST temperature at the bottom interface during reset is nearly independent of temperature.

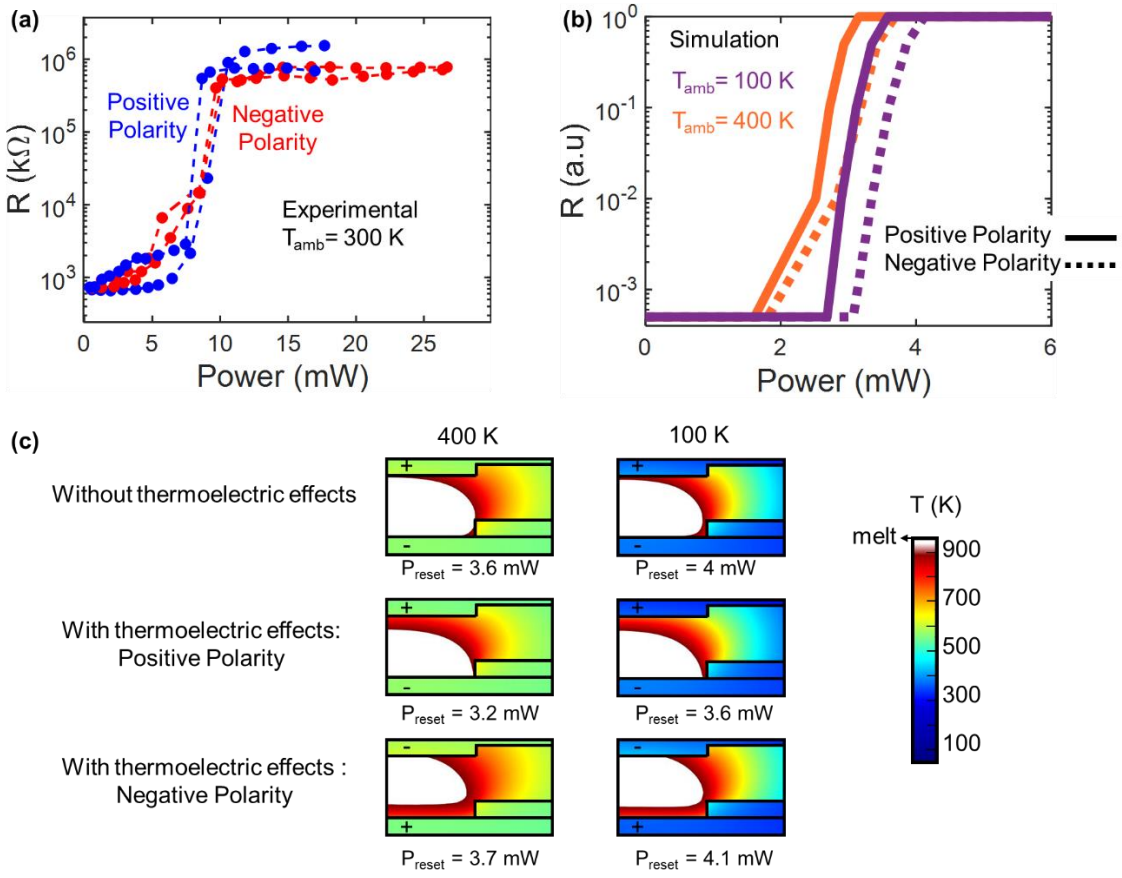

Fig. S1. (a) Experimental results for positive (blue) and negative (red) voltage bias (on the top electrode) at 300 K. The power ratio between the negative and positive polarity is ~1.1. (b) Simulations for positive (solid line) and negative (dashed line) polarity at 100 K (purple) and 400 K (orange). The power ratio between the negative and positive polarities is ~1.15. (c) Simulated temperature maps during reset with and without thermoelectric effects at 100 K and 400 K ambient temperature.

Section 4 – Transient resistance measurement to extract electrical conductivity of melted GST and thermal time constant

R_{trans} is the measured transient resistance during a reset pulse (Fig. S2a). Here the measurement was performed with high power pulse to achieve full reset. The measurement was applied on a nominal 175 nm via diameter with GST thickness of ~ 50 nm. The obtained minimum R_{trans} is 95 Ω, and σ was calculated by considering the device dimensions, as follows (assuming the entire confined volume is melted, which sets a lower bound to σ).

$$\sigma \sim t_{GST}/(R \cdot d_{via}^2) = 50 \cdot 10^{-9}\ \text{m} / (95\ \Omega \cdot 175^2 \cdot 10^{-18}\ \text{m}^2) \sim 2 \cdot 10^4\ \text{S/m}$$

where t_{GST} is the thickness and d_{via} is the via diameter. Our results are in good agreement with melt resistance measurements by Cil *et al.*[7]

From R_{trans} measurements, the thermal time constant, τ_{th}, can be estimated. τ_{th} is the time it takes for a specific GST volume to be melted, and from Fig. S2b, it can be observed that τ_{th} is roughly unchanged with ambient temperature. The transient measurement also confirms that after 20 ns the device reached thermal steady state.

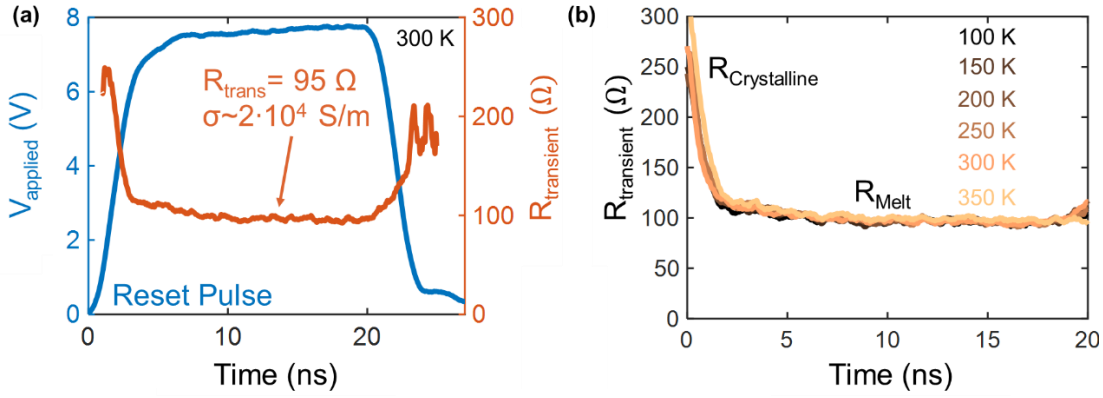

Fig. S2. (a) Transient resistance measured during reset pulse at 300 K to evaluate electrical conductivity of the melt ~$2 \cdot 10^4$ S/m. (b) Transient resistance measured during reset pulse at varying ambient temperatures. The thermal time constant is similar for all ambient temperatures.

We also compared the measured current transient to electro-thermal simulations, which capture the thermal transient with varying ambient temperatures. The transient response is visible thanks to the change in electrical resistivity between the crystalline phase and the melted GST.[7]

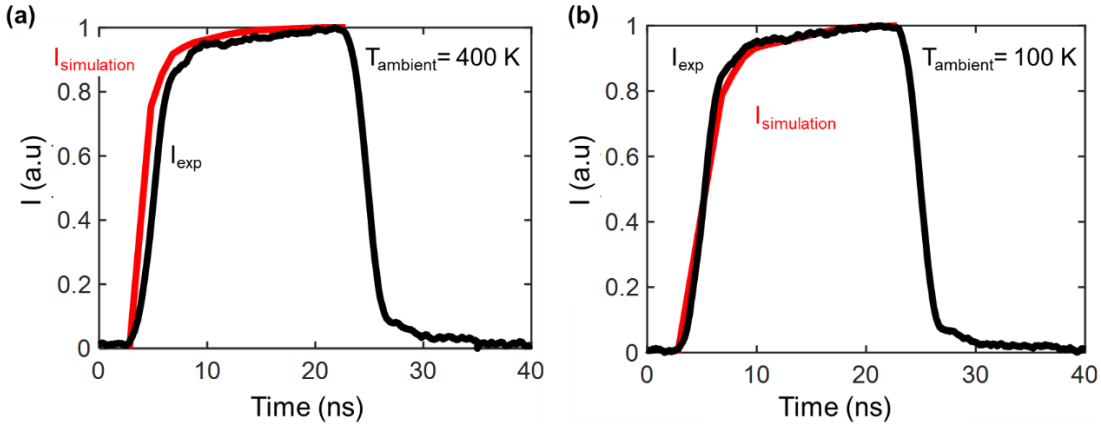

Fig. S3. (a), (b) Simulation and experimental transient current during a reset pulse at 400 K and 100 K ambient temperature, respectively.

Section 5 – Effect of varying via size

This section shows the scaling trend of thermal resistance (reset power dependence on temperature) with varying via size. Fig. S4 shows the read resistance after reset vs. (a,c) power and (b,d) current at different ambient temperatures for two additional via diameters, nominal 200 nm [Fig. S4(a,b)] and nominal 125 nm [Fig. S4(c,d)]. The larger via (200 nm) exhibits a slight shift in the minimum power (and current) for reset at different ambient temperatures, whereas the smaller one (125 nm) presents almost constant reset power (and current) values. Electro-thermal simulations (Fig. S5) show the same scaling trend of ambient temperature vs. reset power. As the via size of a confined cell increases, its thermal behavior changes because more heating occurs at the bottom electrode (BE) and the surrounding of the confined area. As a result, the surrounding interfaces become less dominant in determining the total thermal resistance of the device.

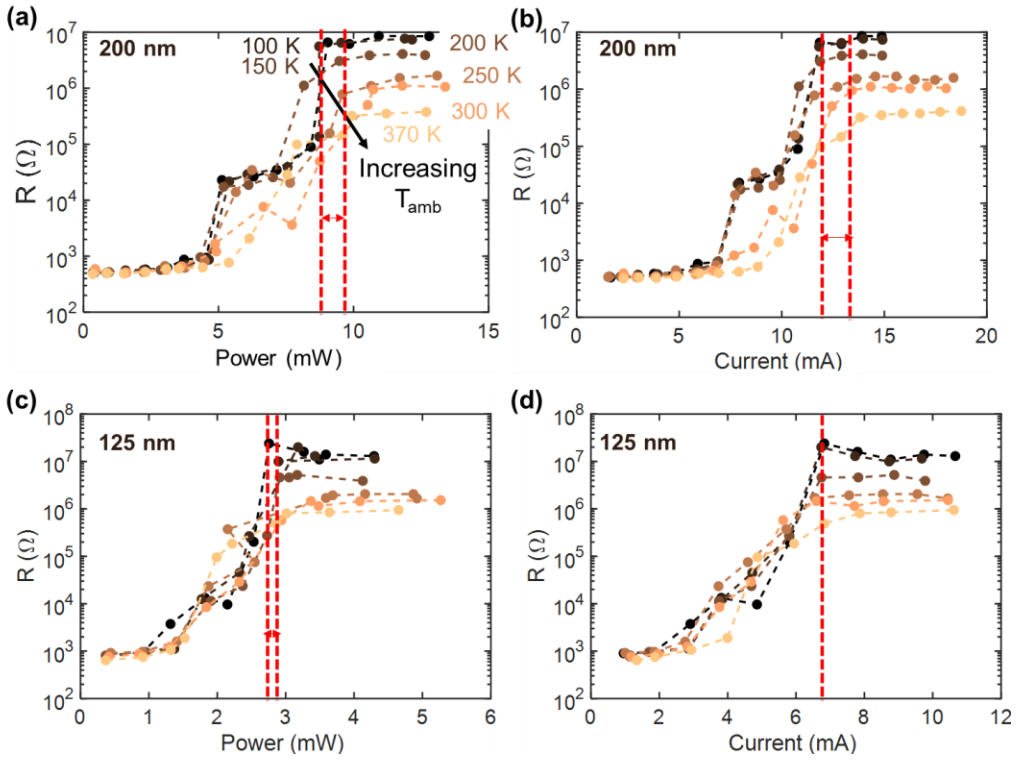

Fig. S4. Final (read) resistance vs. (a,c) power or vs. (b,d) current for varying ambient temperatures in confined PCM devices with nominal via diameter of (a,b) 200 nm and (c,d) 125 nm. Gradual color scale represents increasing ambient temperature, from 100 K (black) to 370 K (light orange). As the via diameter increases, the minimum reset power and current (marked with red dashed lines) become more temperature-dependent.

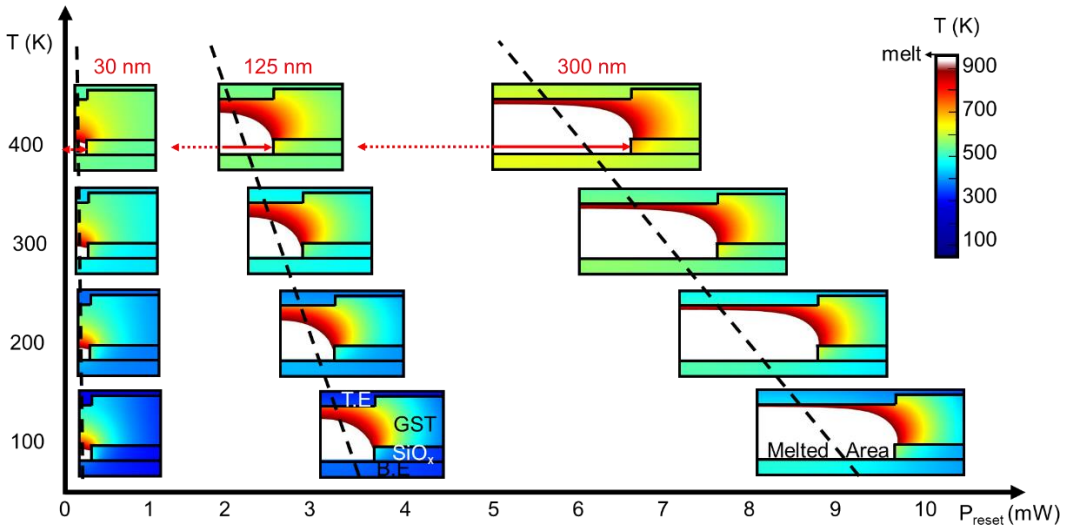

Fig. S5. Electro-thermal simulations of confined PCM devices (half-cell, around the vertical axis of symmetry) with varying via diameter at different ambient temperatures (y-axis) and applied reset power (x-axis). The red arrows represent the via diameter and the color bar represents the temperature during the reset pulse. As vias diameter increases, interface properties become less dominant and reset power becomes more temperature-dependent (thermal resistance is less T-dependent).

Section 6 – Boundary Conditions of Finite Element Method (FEM) Simulation

Device boundary conditions are described below in Fig. S6.

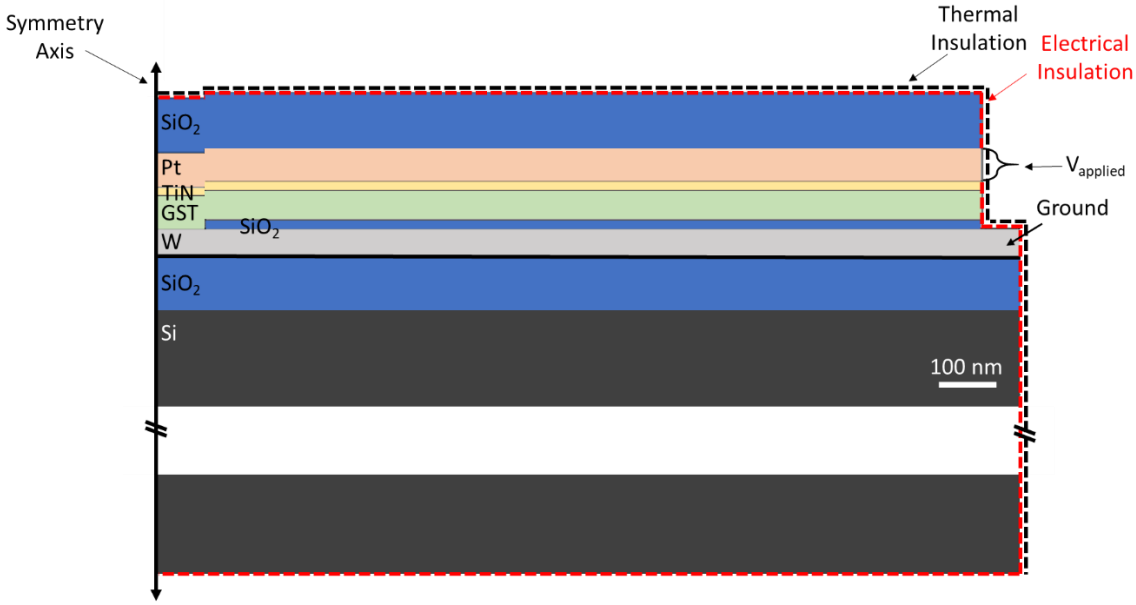

Fig. S6. Boundary conditions of the device. The black dashed line represents the thermal insulation boundaries and the red dashed line represents the electrical insulation boundaries.

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