Effect of Top-Gate Dielectric Deposition on the Performance of Indium Tin Oxide Transistors

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***Abstract*— We report ultrathin (∼4 nm) channel indium tin oxide (ITO) transistors, comparing different precursors for atomic layer deposition (ALD) of the Al_2O_3 top-gate dielectric, and analyze the role of dielectric deposition on transistor performance and gate bias stress stability. Water-based ALD leads to very negative threshold voltage (V_T), with devices remaining in the on-state. In contrast, both ozone and O_2-plasma precursors yield devices that can turn off, but ozone-based ALD devices have less negative V_T shift at short channel lengths, and relatively more positive V_T at all channel lengths. We achieve maximum drive current, $I_{max} \approx 260$ μA/μm at $V_{DS} = 1$ V, on/off current ratio of $>10^{10}$ (limited by the instrument's noise floor) for $L \approx 700$ nm ozone-Al_2O_3 top-gated transistors. Across multiple devices, the effective mobility is ∼42 $cm^2V^{-1}s^{-1}$ and contact resistance is ∼376 $\Omega \cdot \mu$m. The transistors also show good gate bias stability with normalized V_T shift of +0.12 $V(MV/cm)^{-1}$ at gate stress field >3 MV/cm, a ∼3× improvement *vs.* our previous reports of uncapped ITO transistors.**

***Index Terms*— ITO, transistors, atomic layer deposition, effective mobility, contact resistance, bias stress stability.**

I. Introduction

OXIDE semiconductors are compatible with back-end-of-line (BEOL) processing (≤ 500 °C) [1] and monolithic three-dimensional (3D) integration due to their large-scale, low-temperature deposition methods [2], [3], [4], [5]. They are promising candidates as channel materials for field-effect transistors (FETs), due to high drive currents and low off-state currents [2], [3], [6], [7]. Recently, ultra-short channel (∼8 nm) 2.5 nm thin In_2O_3 FETs have shown ∼3 mA/μm drive currents, but they suffer from poor on/off current ratio $<10^2$ [4]. On the other hand, indium gallium zinc oxide (IGZO) devices have demonstrated high on/off current ratio of $\sim10^{12}$ but lower on-state current ∼6 μA/μm [5]. Among this family of materials, indium tin oxide (ITO) transistors have shown both good on- and off-state performance, with effective mobility $\mu_{eff} \sim 55$ $cm^2V^{-1}s^{-1}$ [2] and high on/off current ratio $\sim10^{11}$ [3], [8]. However, almost all ITO transistors have back-gated (BG) structures with no channel encapsulation. Thus, the effect of top dielectric deposition on the performance and stability of ITO FETs remains unexplored.

In this work, we fabricate top-gated (TG) ITO transistors with three different precursors: H_2O, O_2-plasma, and ozone (O_3), for atomic layer deposition (ALD) of the Al_2O_3 TG dielectric. We compare the role of the TG dielectric deposition on device behavior, under DC measurements and positive gate bias stress. In doing so, we determine the optimum precursor for Al_2O_3 top dielectric deposition on ITO channels, based on parameters like threshold voltage (V_T), on/off current ratio, mobility, drive current, minimum subthreshold swing and V_T stability.

II. Fabrication and Measurement

The cross-sectional schematic of a device along with the fabrication steps are shown in Fig 1(a). First, we deposit ∼4 nm thick ITO channels by radio frequency (RF) magnetron sputtering on SiO_2 (95 nm)/p^{++} Si substrates, which are used as global back-gates for initial BG measurements. The ITO deposition is done at room temperature with 100 W RF power, 5 mTorr deposition pressure, and 9:1 Ar:O_2 ratio. The channel region is patterned by lift-off or wet etching in diluted HCl (1.7%). Next, we e-beam evaporate and lift-off Ni (40 nm)/Au (20 nm) as source/drain contacts. For the TG dielectric, ALD of ∼30 nm Al_2O_3 film is done at 200 °C, with three different precursors: H_2O, O_2-plasma, and ozone (O_3). Then, we e-beam evaporate and lift-off Ti (3 nm)/Pd (80 nm) as TG metal contact, before opening the source/drain contact pads by wet etching of Al_2O_3. The temperature remains ≤ 200 °C throughout all fabrication steps.

We fabricate transfer length method (TLM) structures with transistors of different channel lengths ($L \sim 0.7$, 1.6, 2.8, 4.7, 7.3, and 9.8 μm). Figs. 1(b,c) show an optical and a scanning electron microscope image of a TLM before and after TG dielectric and metal deposition, respectively. Fig. 1(d) shows

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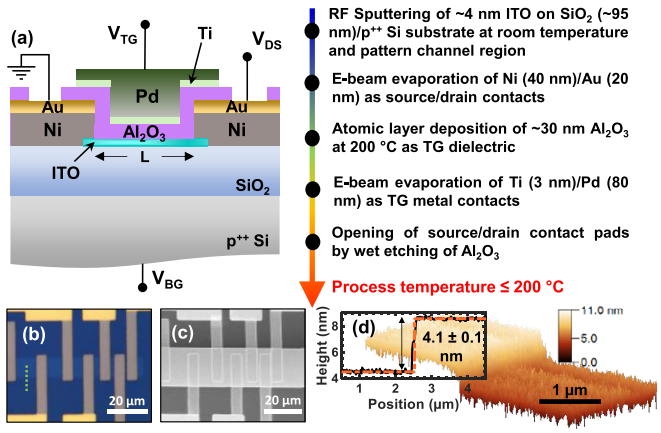

Fig. 1. **(a)** Schematic cross-section of the device structure and fabrication process flow of ITO transistors. **(b)** Optical image (before TG dielectric and metal deposition) and **(c)** scanning electron microscopy image (after TG dielectric and metal deposition) of transfer length method (TLM) structure. **(d)** Atomic force microscopy image across the green dotted line shown in (b); orange dashed line fitting the height profile (inset) shows the ITO channel thickness.

the atomic force microscopy profile across the green dotted line in Fig. 1(b), confirming the ITO thickness ~4 nm. All electrical measurements were done at room temperature, in air, using a probe station with a Keithley 4200-SCS.

III. Results and Discussion

A. Back-Gated (BG) Measurements

For initial analysis, we performed BG measurements using the p^{++} Si substrate as a back-gate. The gray and blue curves in Fig. 2 show the BG transfer characteristics (I_D-V_{BG}) of the uncapped and Al_2O_3-capped devices, respectively, for two channel lengths ($L \sim 1.6$ μm and 9.8 μm). The effect of ALD capping is shown with the three different precursors, H_2O, O_2, and O_3, one in each panel of Fig. 2. The transfer curves for all uncapped, as-deposited samples are similar, with similar V_T. After ALD of H_2O-Al_2O_3 the V_T strongly shifts negatively, and the devices lose BG modulation [Fig. 2(a)]. This conductive channel could be caused by H-doping with residual H from the H_2O precursor, or by the highly reactive trimethylaluminum precursor stripping off chemisorbed oxygen or -OH groups from the oxide channel, generating oxygen vacancies which donate free electrons [9], [10]. However, after O_2-plasma and O_3-based ALD, the transistors retain good BG modulation, suggesting passivation of oxygen vacancies or reintroduction of -OH groups into the channel, unlike H_2O-based ALD [9]. For O_2-plasma ALD, V_T remains close to the as-deposited case [Fig. 2(b)], while O_3-ALD shifts the V_T positively, closer to 0 V [Fig. 2(c)]. A control experiment with the same number of *only* oxidant (O_2 and O_3) pulses revealed that both types of reactants shift the V_T positively, and thus the duration, order, and number of O_2 or O_3 oxidant cycles may be tuned to achieve a desired V_T.

B. Top-Gated (TG) Measurements

Fig. 3(a) shows the TG transfer characteristics (I_D-V_{TG}) of 1.6 μm devices with the three types of Al_2O_3 as TG dielectric. As for the BG measurement, the H_2O-precursor transistors show no TG modulation. On the other hand, O_2 and O_3-Al_2O_3 devices are modulated by the TG (like the BG), but the O_2-plasma Al_2O_3 device displays more negative V_T (−1.1 V *vs.* 0.03 V) and degraded minimum subthreshold

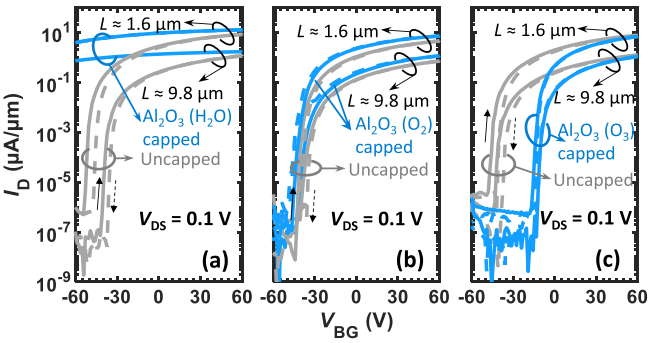

Fig. 2. Back-gated (BG) transfer characteristics for ITO transistors (with $L \sim 1.6$ and 9.8 μm) before (gray) and after (blue) capping with Al_2O_3 by ALD using **(a)** H_2O, **(b)** O_2-plasma, and **(c)** O_3 precursor. Solid and dashed small arrows indicate the voltage sweep directions and correspond to the solid and dashed curves, respectively. For all measurements, BG leakage currents were $< 10^{-5}$ μA/μm.

swing (~430 mV/dec *vs.* ~230 mV/dec). Fig. 3(b) shows I_D-V_{TG} curves for O_2- and O_3-Al_2O_3 devices with $L \approx 700$ nm. Here, the O_3-Al_2O_3 device shows $I_{max} \approx 260$ μA/μm at $V_{TG} = 20$ V and $V_{DS} = 1$ V, on/off current ratio $>10^{10}$ (limited by the noise floor of the instrument), extrinsic field-effect mobility $\mu_{FE,ext} \approx 38$ cm^{2}V^{-1}s^{-1} and $V_T = -1.6$ V. The $\mu_{FE,ext}$ and V_T are extracted at peak transconductance. Note, at this shorter channel length, the V_T shifts more negatively for O_2-plasma Al_2O_3 device (−7.9 V *vs.* −1.6 V for O_3), together with increased hysteresis and drain-induced barrier lowering (|DIBL| ≈ 261 ± 182 mV/V for O_2-plasma *vs.* 128 ± 66 mV/V for O_3). Such degradation may be explained by the oxygen vacancies in the channel and under the contacts, acting as dopants and defect centers, which can cause charge trapping and affect the semiconductor capacitance. However, this needs to be investigated in more detail in future studies.

Figs. 3(c,d) show output characteristics (I_D-V_{DS}) for ~700 nm long devices with O_2-plasma and O_3-based Al_2O_3 TG dielectric, respectively. The O_3-Al_2O_3 device has a less negative $V_T \approx -3$ V *vs.* −10 V for O_2-plasma. In addition, for the same TG overdrive voltage ($V_{TG} - V_T = 7$ V) at $V_{DS} = 4$ V, the drive current of the O_3-Al_2O_3 sample is almost double that of the O_2-Al_2O_3 device (498 μA/μm *vs.* 266 μA/μm).

Fig. 4(a) displays V_T roll-off *i.e.* decreasing V_T at shorter channel lengths, ostensibly due to oxygen scavenging at the contacts [5], [11] for both O_2 and O_3-Al_2O_3 samples. The O_3 precursor sample shows less V_T roll-off (−4.4 V) compared to the O_2-plasma (−15.9 V), which could be due to the passivation of a dissimilar number of oxygen vacancies in the channel during ALD. Here, the V_T roll-off is the V_T difference between the longest (~9.8 μm) and shortest (~700 nm) channels. Notably, $V_T > 0$ V for the O_3-Al_2O_3 sample down to ~1.6 μm channel length, only becoming negative ($V_{T,avg} \approx -2.2$ V) for the shortest channel (~700 nm). On the other hand, the average V_T's for the O_2-Al_2O_3 devices remain negative for all channel lengths. Further reduction of the dielectric and channel thickness could achieve a positive V_T with turn-on voltage close to 0 V, at the expense of lower on-state current due to the thinner channel [12].

Fig. 4(b) shows the plot for total resistance (R_{Total}, averaged over 8 to 10 devices at each channel length) *vs.* channel length L for both O_2 and O_3-Al_2O_3 samples. This allows the extraction of contact resistance (R_C) and effective mobility (μ_{eff}) at a given electron density, $n \approx 2.6 \times 10^{13}$ cm^{-2}, estimated as

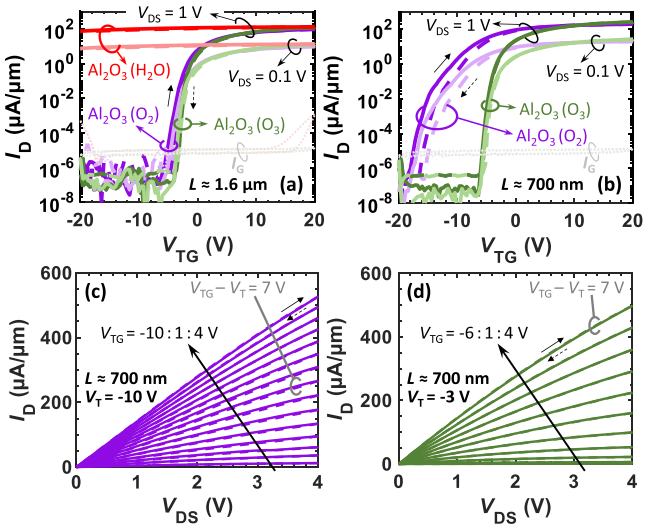

Fig. 3. Top-gated (TG) transfer characteristics for **(a)** $L \approx 1.6$ μm and **(b)** $L \approx 700$ nm. For all measurements, TG leakage currents (I_G) were $< 10^{-5}$ μA/μm. **(c)** Output characteristics (I_D-V_{DS}) for ~700 nm devices with O_2 and **(d)** O_3-Al_2O_3 TG dielectric. Solid and dashed small arrows mark voltage sweep directions and correspond to the solid and dashed curves, respectively. Purple and green are used to denote O_2-plasma and ozone (O_3) Al_2O_3 samples, respectively, in all panels.

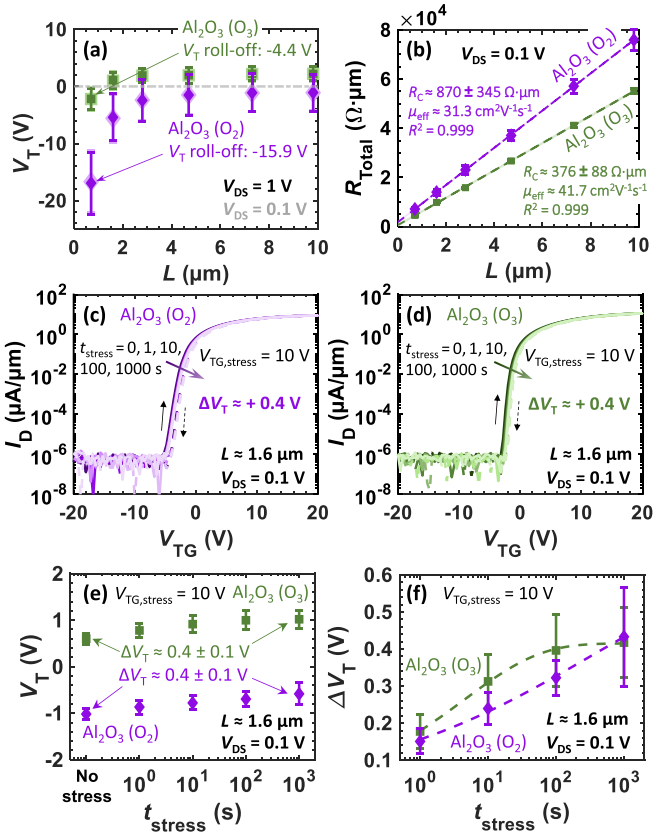

Fig. 4. Plots of **(a)** threshold voltage V_T *vs.* channel length L, **(b)** total resistance R_{Total} *vs.* L at electron density, $n = 2.6 \times 10^{13}$ cm^{-2}. Error bars represent the standard deviation among 8 to 10 devices at each channel length. Insets in (b) list the estimated contact resistance R_C (from the vertical axis intercept of the linear fit) and the effective mobility, μ_{eff}, whereas R^2 denotes the goodness of fit. **(c)** Positive bias stress analysis at $V_{TG,stress} = 10$ V for ~1.6 μm devices with O_2 and **(d)** O_3-Al_2O_3 TG dielectric. Solid and dashed small arrows indicate the voltage sweep directions and correspond to the solid and dashed curves, respectively. Evolution of **(e)** V_T and **(f)** V_T shift, ΔV_T, *vs.* stress time, t_{stress} for $V_{TG,stress} = 10$ V. Error bars in (e, f) mark the variability among 5 devices. Dashed lines in (f) are fit to the stretched-exponential model in [14]. Purple and green are used to denote O_2-plasma and ozone (O_3) Al_2O_3 samples, respectively, in all panels.

$n = C_{TG}(V_{TG} - V_T)/q$, where $C_{TG} \approx 0.28$ μF/cm^2 for O_2-Al_2O_3 and 0.29 μF/cm^2 for O_3-Al_2O_3 is the top-gate capacitance and q is the elementary charge. The O_3-Al_2O_3 sample shows lower $R_C \sim 376$ Ω · μm and higher $\mu_{eff} \sim 41.7$ cm^{2}V^{-1}s^{-1} compared to the O_2-Al_2O_3 sample. The difference in the R_C and mobility values for the two samples is also present in the BG measurement before ALD capping, as evident from the lower drive current of the O_2-plasma sample before ALD [Fig. 2(b)]. Before ALD capping, the samples have R_C and μ_{eff} of ~495 Ω·μm and ~28.6 cm^{2}V^{-1}s^{-1} [Fig. 2(b)] *vs.* ~313 Ω·μm and ~45.2 cm^{2}V^{-1}s^{-1} [Fig. 2(c)] respectively, at $n = 1.1 \times 10^{13}$ cm^{-2}. This difference could be due to variation in as-deposited ITO films and/or Ni contacts, possibly caused by different chamber conditions during different runs. Notably, the Al_2O_3 capping introduces further changes in these parameters, possibly due to passivation of oxygen vacancies in the ITO film during ALD.

Figs. 4(c,d) show the positive bias stress stability of ~1.6 μm long O_2 and O_3-Al_2O_3 samples at a TG bias stress field of ~3.33 MV/cm. Interestingly, both samples show similar V_T shift ($\Delta V_T \approx +0.4$ V) due to positive bias stress. This corresponds to a positive normalized V_T shift of 0.12 V(MV/cm)$^{-1}$, which is ~3× more stable compared to uncapped ITO devices under similar back-gate stress field reported in our prior work [13]. Figs. 4(e,f) show the evolution of V_T and ΔV_T with stress time (t_{stress}) averaged across 5 devices each from O_2 and O_3-Al_2O_3 samples. The dashed lines in Fig. 4(f) are the stretched-exponential model of ΔV_T time dependence [14], based on charge trapping and redistribution from the channel interface into the dielectric. The model is $\Delta V_T = \Delta V_{T0}\{1 - \exp[-(t/\tau)^{\beta}]\}$, where ΔV_{T0}, τ, and β represent ΔV_T at infinite time, the average trapping time of electrons, and a fitting exponent, respectively. In our work, these parameters are ~0.6 V, 314 s and 0.21 for O_2-Al_2O_3 and ~0.42 V, 4.4 s and 0.39 for O_3-Al_2O_3, respectively. During bias stress testing, we took DC measurements of the transfer curves, which took ~14 s with no additional hold or delay time in between the stress and measurement. The stress time was accumulated over all cycles.

IV. Conclusion

We report top-gated ITO transistors with good $R_C \sim 376$ Ω · μm and $\mu_{eff} \sim 42$ cm^{2}V^{-1}s^{-1}. We achieve $I_{max} \approx 260$ μA/μm at $V_{DS} = 1$ V in a ~700 nm long channel with O_3-based Al_2O_3 as the top dielectric. We show that, both O_3 and O_2-plasma precursors during the ALD of the top-gate dielectric produce bias stress stable devices. Using O_3 precursor over O_2-plasma demonstrates the advantage for minimizing the V_T roll-off after ALD as well as reducing short channel effects. These results are important for ITO channel transistor applications in BEOL and 3D integration. They also open a pathway towards enhancing oxide transistor performance by channel length scaling and improved gate control, *i.e.* dual-gating or gate-all-around structures.

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