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Self-Aligned Nanotube–Nanowire Phase Change Memory

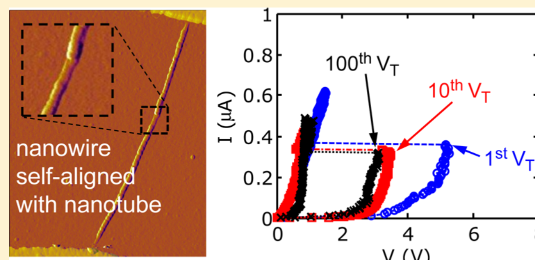
Feng Xiong,[†,‡,§] Myung-Ho Bae,[†,‡,⊥,#] Yuan Dai,[†,‡,#] Albert D. Liao,[†,‡] Ashkan Behnam,[†,‡] Enrique A. Carrion,[†,‡] Sungduk Hong,[†,‡] Daniele Ielmini,[∥] and Eric Pop*[,†,‡,§]

[†]Micro and Nanotechnology Lab, [‡]Department of Electrical and Computer Engineering, and [§]Beckman Institute, University of Illinois, Urbana–Champaign, Illinois 61801, United States

[∥]Dipartimento di Elettronica e Informazione, Politecnico di Milano, 20133 Milano, Italy

Supporting Information

ABSTRACT: A central issue of nanoelectronics concerns their fundamental scaling limits, that is, the smallest and most energy-efficient devices that can function reliably. Unlike charge-based electronics that are prone to leakage at nanoscale dimensions, memory devices based on phase change materials (PCMs) are more scalable, storing digital information as the crystalline or amorphous state of a material. Here, we describe a novel approach to self-align PCM nanowires with individual carbon nanotube (CNT) electrodes for the first time. The highly scaled and spatially confined memory devices approach the ultimate scaling limits of PCM technology, achieving ultralow programming currents (~0.1 μA set, ~1.6 μA reset), outstanding on/off ratios (~10^3), and improved endurance and stability at few-nanometer bit dimensions. In addition, the powerful yet simple nanofabrication approach described here can enable confining and probing many other nanoscale and molecular devices self-aligned with CNT electrodes.



KEYWORDS: *Phase change memory, nanowire, self-aligned, carbon nanotube, interconnects*

Computing and data storage based on spin,[1,2] resistive switching,[3,4] or phase change[5−13] have received considerable attention as charge-based electronics approach their fundamental scaling limits, particularly due to charge leakage and power dissipation issues.[14] Phase-change materials (PCMs), such as the chalcogenide $Ge_2Sb_2Te_5$ (GST), are particularly interesting for applications in electrical or optical data storage[5−13] and reconfigurable electronics.[15] Unlike conventional charge-based electronics, PCM-based devices store data as the state of the material that can be reversibly switched between a high-resistance amorphous and a low-resistance crystalline phase. This behavior renders them immune to leakage as nonvolatile memory for low-power electronics, and relatively impervious to radiation damage for remote terrestrial or space applications. PCM switching is induced by Joule heating through voltage pulses for electrically programmable PCM devices.[6−13] However, such devices have historically required relatively high-programming current (0.1–0.5 mA) and power (~0.5 mW).[6,7] To address this challenge, the dimensions of the programmable bit could be reduced by laterally confining[16] it into nanowires (NWs)[8−10] or by contacting it with ultrasharp electrodes like carbon nanotubes (CNTs).[11−13] NWs confine the bit in the cross-plane perpendicular to the current flow, while CNTs can contact very small bit dimensions commensurate with their ~2 nm diameter.

In this study, we present a method to self-align PCM nanowires with CNT electrodes for the first time, achieving confinement of highly scaled PCM bits in three dimensions. Such devices display ultralow power operation and electrical characteristics (e.g., on/off ratio) that approach the fundamental scaling limits of the PCM. The simple nanofabrication technique does not require lithography to self-align PCM nanowires with CNT electrodes and can be easily adapted to confine and probe many other nanoscale materials and devices.

Figure 1 presents a schematic of our approach and atomic force microscopy (AFM) images of a device at different fabrication stages. We begin with a CNT spanning two Pd electrodes[17,18] on a SiO_2/Si substrate, as shown in Figure 1a,b and further described in the Methods and Supporting Information. CNTs are either single-wall (metallic or semiconducting) or small-diameter (d < 5 nm) multiwall, and both types can be used in the fabrication and devices described here. We spin a thin layer of polymethyl methacrylate (PMMA), typically ~50 nm onto the device (Figure 1c). We then apply a voltage across the Pd pads in vacuum (~10^{-5} Torr), flowing current through the CNT such that localized Joule heating along its length[13,17] causes the PMMA covering it to evaporate,[19,20] leaving behind a narrow trench self-aligned with the CNT (Figure 1d,e). This process is done in vacuum to prevent electrical breakdown of CNTs at this stage, since the breakdown voltage of CNTs in vacuum is typically a factor of 2–3× greater than in air for a given CNT length.[17]

We then create a nanogap (~20–150 nm) in the exposed CNT by electrical breakdown[11,17] at high bias in air under Ar flow (Figure 1f). The size of this nanogap can be controlled by

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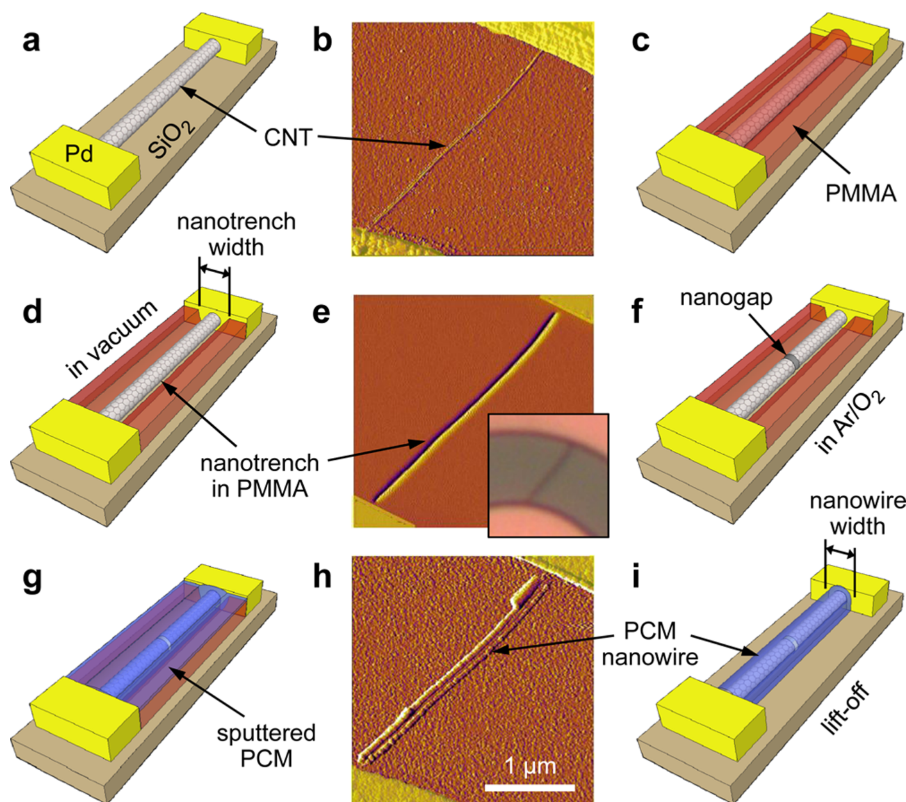

Figure 1. Schematics and atomic force microscopy (AFM) imaging of self-aligned device. (a) CNT between two Pd electrodes. (b) False color AFM of a CNT with length $L \approx 3.1$ μm and diameter $d \approx 2.2$ nm. (c) The CNT device is coated with a thin layer (∼50 nm) of PMMA. (d) Current flow in the CNT leads to Joule heating and nanotrench formation along it as the PMMA evaporates; this procedure is performed in vacuum (10^{-5} Torr) to prevent CNT breakdown. (e) AFM imaging of nanotrench (∼90 nm wide) in PMMA. Inset shows nanotrench is visible under the optical microscope, enabling quick and easy detection. (f) CNT nanogap is formed by electrical cutting under Ar/O_2 flow, which enables localized breakdown by oxidation. (g) PCM deposition covers the device and fills the nanogap and nanotrench. (h,i) AFM imaging and schematic of self-aligned NW with CNT electrodes obtained after PMMA lift-off. Some devices were further encapsulated with a ∼10 nm layer of evaporated SiO_2.

the partial pressure of Ar/O_2 available,[21] although nanogaps can also be created by other techniques such as electron-beam "cutting" of CNTs, for higher throughput.[22] We then sputter ∼10 nm of GST over the device, filling the nanogap and nanotrench as shown in Figure 1g. We lift-off the remaining PMMA (see Methods), leaving behind a GST NW that spans the nanogap and is perfectly aligned with the CNT electrodes (Figure 1h,i). The memory bit is formed by the small amount of GST confined longitudinally in the nanogap and laterally by the NW width. Most devices were capped with ∼10 nm evaporated SiO_2 to protect the GST from oxidation; some were left uncapped to characterize the effect of this encapsulation on device reliability at such diminutive bit dimensions.

The AFM image and electrical characteristics of several devices are shown in Figure 2 (also see Supporting Information Figure S5). Figure 2b shows current−voltage ($I-V$) characteristics under DC current sweep, demonstrating memory SET switching from the high resistance amorphous phase ($R_{OFF} \approx$ 2.5 GΩ) to the low-resistance crystalline phase ($R_{ON} \approx$ 1.3 MΩ). The SET switching is initiated at a threshold voltage (V_T) through a field-induced transition of the amorphous phase;[23] Joule heating then crystallizes the bit at ∼150 °C into the conductive state. The device V_T decreases by 20−30% after the first few switching cycles (Figure 2b and Supporting Information Figure S6), which is consistent with previous reports.[11,12] This "burn-in" is beneficial as it stabilizes the memory bit and allows lower power operation in the long run. Reversible memory switching is achieved with pulsed operation and shown in Figure 2c. The bit is reamorphized (RESET) with a current pulse which heats up the crystalline GST (c-GST) to its melting point (∼620 °C) then quenches it back to a disordered amorphous GST (a-GST) state during the short falling edge of the pulse. This device has $R_{OFF}/R_{ON} \approx 2000$, effectively approaching the intrinsic resistivity ratio of a-GST and c-GST ($\rho_a/\rho_c \approx 10^3-10^4$) much closer than previously possible.[11,12]

The self-aligned structure presents several benefits allowing us to approach the fundamental limits of switching in such small PCM bits. The narrow constriction of the self-aligned NW (Figure 2a inset) enables the ultrahigh off/on ratio by eliminating parasitic leakage paths around the small PCM bit. The NW constriction also improves device endurance (Figure 2d) compared to previous results with CNT electrodes,[11,12] by limiting the size of the so-called crystalline "halo" that can form around the bit region[24] after several switching events. The programming currents are reduced by ∼100× compared to industrial state of the art[16,25] by the use of CNT electrodes which have much smaller diameter (∼2 nm) than typical metal electrodes (∼20−80 nm); in addition, the combination of CNT electrodes and narrow NW constriction further reduces programming current by 3−5× with respect to devices which utilized CNT electrodes alone.[11]

Figure 2e shows that both memory states are stable under constant 1 V readout for 10^4 s at room temperature (Figure 2e), equivalent to 10^{11} cycles of 100 ns read operations. Another important figure of merit for PCM devices is their stability over time, t; the a-GST resistance can drift as $R(t) = R(t_0)(t/t_0)^\alpha$ likely

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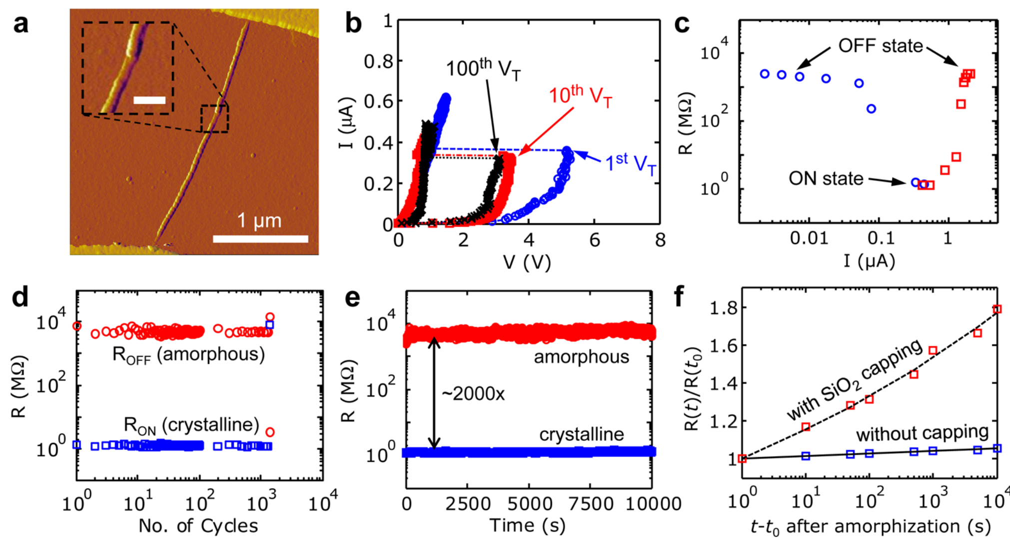

Figure 2. Device electrical characteristics. (a) AFM image of a self-aligned NW with CNT electrodes of $d \approx 2.5$ nm. The GST nanowire is ~40 nm wide, ~10 nm tall, and capped by ~10 nm SiO_2. The nanogap size is difficult to measure within the nanotrench by AFM but can be estimated from the threshold field[11] (~50−100 V/μm) and the threshold voltage (~3 V) to be ~30−60 nm. Inset zoom-in shows the nanogap region (scale bar 150 nm). (b) Electrical characteristics of the 1st, 10th, and 100th SET switch, showing the threshold voltage stabilizes at $V_T \approx 3.2$ V. (c) Resistance switching after a series of current pulses with increasing amplitude. SET (RESET) pulses have 300 ns (100 ns) width and rising (falling) edges of 50 ns (2 ns). The SET (RESET) current is ~0.4 μA (~1.9 μA). The ratio R_{OFF}/R_{ON} = 2.5 GΩ/1.3 MΩ, nearly ~2000×. (d) Endurance test over nearly 1500 cycles of operation. (e) On and off states are stable for 10^4 s under a constant 1 V readout, equivalent to 10^{11} read operations with 100 ns pulses. (f) Normalized resistance drift in off-state after reamorphization without (blue squares) and with (red squares) SiO_2 capping. The solid and dashed linear fit shows drift coefficient $\alpha \approx 0.006$ and 0.062, respectively. Panels (b−e) are from the same device; panels (a,f) are from other representative devices.

due to structural relaxation[26−28] with typical drift coefficient α = 0.05−0.1. In Figure 2f, we find that the drift coefficient of a self-aligned NW without capping is extremely low (~0.006), and it is slightly higher (~0.062) with ~10 nm of SiO_2 encapsulation, which is consistent with previous findings.[26] The higher drift slope could be due to enhanced mechanical stress in the encapsulated NW[26] or to a change in GST composition affecting the band structure and the drift properties.[28] Coupled with the extremely high off/on ratio, such low drift coefficients could enable multilevel memory applications even at the most reduced bit dimensions.[6,7]

Figure 3a displays the measured R_{ON} and R_{OFF} of all self-aligned devices vs threshold voltage, chosen as the stable V_T after "burn-in" of the first cycles. Out of 102 devices measured, two exhibited R_{OFF}/R_{ON} ~2000, approximately ten had R_{OFF}/R_{ON} > 1000, and the overall average was $R_{OFF}/R_{ON} \approx 452$ (see histogram in Supporting Information Figure S7). The measured resistance is effectively that of the PCM bit in the nanogap, which is more resistive than the CNT electrodes regardless of phase. Thus, we can expect a linear scaling of R versus V_T, both being proportional to the nanogap size formed between the CNT electrodes,[11,23] as explained below.

The solid (dashed) line in Figure 3a is a linear fit of R_{ON} (R_{OFF}) versus V_T with a slope 0.5 MΩ/V (110 MΩ/V) and intercept 725 kΩ (630 MΩ). The y-intercept of the on-state is the average parasitic series resistance (R_S) introduced by the CNT, the CNT-GST contacts, and CNT-Pd contacts. We found $R_S \approx 725$ kΩ for the on-state, which is larger than the typical resistance of our CNTs before processing (~100 kΩ).[13,17] This suggests that the GST deposition introduces some CNT defects,[13] and that both CNT-Pd and CNT-GST contact resistances could be improved, leading to potentially higher and more consistent R_{OFF}/R_{ON} ratios. The presence of these series resistance components also explains some of the variability seen between our different devices (Figure 3a and Supporting Information Figure S7), which could be better controlled in future work by using gentler GST deposition techniques (e.g., by atomic layer deposition[29]) and by improving the CNT contacts to GST and to metal electrodes.

The slope of the linear fits in Figure 3a can be used to estimate the approximate bit cross-sectional area A as follows. The measured resistance of the bit from pad-to-pad is

$$R_{ON,OFF} = R_S + \rho_{c,a}\frac{L}{A} \tag{1}$$

where R_S was defined above, $\rho_{c,a}$ is the resistivity of the GST bit (crystalline or amorphous), and L and A are the length of the PCM bit (the nanogap size) and its effective cross-section, respectively. We note that this effective cross-section is not necessarily the NW cross-section, nor the CNT cross-section, but most likely lies between the two. We can also express the measured threshold voltage as

$$V_T = FL + IR_S \tag{2}$$

where $F \sim 50−100$ V/μm is the threshold field for switching in the nanogap[11] and IR_S is the total parasitic voltage drop at the threshold point. Hence, we can obtain a simple expression linking the measured $R_{ON,OFF}$ and V_T through a linear trend:

$$R_{ON,OFF} = R_S + \left(\frac{\rho_{c,a}}{A}\right)\left(\frac{V_T - IR_S}{F}\right) \tag{3}$$

Thus the slope of the linear fit of R vs V_T is $dR/dV_T \approx \rho/(AF)$, allowing us to estimate an effective cross-sectional area of the bit in both its on and off states. Taking the resistivity of GST in the two states as $\rho_a \sim 1$ Ω·m and $\rho_c \sim 10^{-4}$ Ω·m, respectively, F as given above, and slopes of 0.5 (on-state) and 110 MΩ/V (off-state), we can obtain estimates of the bit area $A_{ON} \approx 2−4$ nm^2 for the on-state and $A_{OFF} \approx 90−180$ nm^2 for the off-state. The average on-state bit area is very similar to the typical CNT cross-sectional area, potentially suggesting conduction through a single GST filament bridging the two CNT electrode tips in

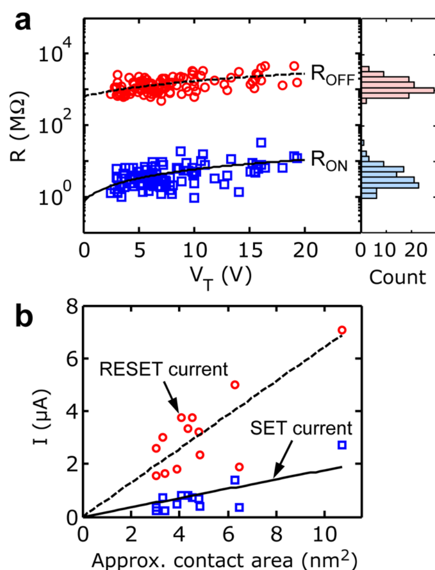

Figure 3. Device statistics and scaling. (a) On and off-state resistance of 102 self-aligned NW-CNT devices studied, plotted against their threshold voltages V_T. The solid and dashed fits suggest approximately linear scaling between R and V_T, both governed by the bit size within the CNT nanogap (also see Figure 2a inset). The y-intercept of the on-state represents the remaining parasitic resistance, and the slopes of both lines can be used to estimate the approximate bit cross-sectional area (see text and Supporting Information). The average $R_{OFF}/R_{ON} \approx 452$ and some devices have ratio ~2000, near the intrinsic limits achievable with the GST material. The right panel shows a histogram of the same data set. (b) SET and RESET programming currents of 13 self-aligned devices suggest approximately linear scaling as a function of CNT electrode tip area (also see Supporting Information). The solid (dashed) line are a fit of the SET (RESET) current with a slope of 0.17 $\mu A/nm^2$ (0.64 $\mu A/nm^2$). The latter is an important figure, representing the expected scaling of RESET current near the fundamental limits of PCM technology.

the nanogap. A similar filamentary-switching was recently proposed for PCM devices with one-sided CNT contacts.[12] The average off-state bit area is slightly smaller than the cross-section of the NWs. Given that the NWs are all ~10 nm tall (the deposited GST thickness), this suggests that the off-state leakage current is spread across approximately 9–18 nm of the width of the NWs (which are all somewhat wider than this).

Figure 3b also finds that the RESET and SET currents scale approximately with the electrode tip area, estimated as $\pi d^2/4$ where d is the CNT diameter. The self-aligned device with 1.7 nm diameter CNT electrodes has $I_{RESET} \approx 1.6\ \mu A$, which represents one of the lowest currents ever measured[11,12] for nanoscale PCM (also see scaling trend in Supporting Information Figures S8 and S9 and surrounding discussion). The estimated energy per bit during SET is ~30 fJ and during RESET ~80 fJ, the latter being limited by the approximately ~30 ns pulse widths used in our setup, which in principle could be reduced by another order of magnitude. Such tiny dimensions and low energy consumption could allow for high-density, energy-saving, solid-state storage for portable devices and data servers.[14]

We now turn to the broader applications of our self-aligned fabrication method. Other than studying the fundamental limits of PCMs, this powerful but simple lithography-free technique could be used to probe other nanomaterials by automatically aligning them with CNT electrodes. For instance, this approach could enable study of precisely positioned nanoparticles,[30] individual molecules[31] or DNA strands.[32] Figure 4a–c shows how the nanotrench width W (and subsequent NW) can be tuned by the power input to the CNT heater during trench formation. Figure 4d shows 17 nanotrench widths as a function of the CNT input power, compared to the results of a computational model (detailed in the Supporting Information). Two examples of other NWs (Au and HfO_x) self-aligned with CNTs through the same process are shown in Figure 4e,f, and more are given in Supporting Information Figure S15.

We have been able to fabricate self-aligned NWs down to ~40-nm wide, and our simulations suggest widths near ~10 nm could be achieved with thinner PMMA, lower background temperature, or the use of pulsed heating (Supporting Information). To be more specific, our simulations (Figure 4d and Supporting Information Figure S14) suggest that the minimum nanotrench width is limited by the PMMA thickness, which in turn is limited by the need to achieve successful lift-off of the nanowire pattern. Thus, if a nanowire is desired, this lower limit may be of the order 20–30 nm. However, if only the nanotrench is used in a future study without the need for lift-off (e.g., filling it with molecules to be electrically probed by the CNT), then nanotrenches as narrow as <10 nm could be achieved, limited only by radial heat flow from the CNT and using ~10 nm thin PMMA layers. Other thermally decomposing resists could also be used instead of PMMA, and such issues along with other optimizations will be explored in future work.

In summary, we developed a novel technique to fabricate sub-50 nm NWs that are self-aligned to CNT electrodes without the need for complex lithography. This enabled us to study PCM devices with bits of a few hundred cubic nanometers, confined by the CNT nanogap and NW width. Such self-aligned PCM devices show ultrasmall power consumption, improved endurance, and extremely high off/on ratios approaching the intrinsic limits of the PCM. The powerful yet simple nanofabrication method could also serve as an excellent platform to study other nanoelectronic and molecular devices and materials self-aligned with CNT electrodes.

Methods. Carbon nanotubes (CNTs) were grown by chemical vapor deposition (CVD) from Fe catalyst on SiO_2 (90 nm)/Si substrates.[17,18] Metal contacts were deposited by successive electron-beam (e-beam) evaporation of Ti/Pd/Au (0.5/20/20 nm). Devices were annealed in vacuum or Ar flow at 300–400 °C for an hour after metal deposition to improve contact resistance. For nanotrench formation, PMMA 495 A2 (from MicroChem) was spun onto the device, usually at 4500 rpm. PMMA thickness was measured by ellipsometry. The nanogaps in CNTs were formed by electrical cutting in air ambient under Ar flow nozzle.[11,17] GST was deposited by DC sputtering under 3 mTorr of Ar flow, with a deposition rate of 0.1 Å/s. GST film thickness (~10 nm) was confirmed by both AFM and X-ray reflectivity (XRR) measurements. DC sputtering power was kept minimal (~6 W) for better lift-off results. Lift-off was performed in acetone solution with mild sonication (5–10 s) typically used to achieve cleaner results. To test for leakage, we also performed control experiments on CNTs without GST, which did not switch reversibly.

Electrical measurements were performed with a Keithley 4200 Semiconductor Characterization System (SCS), a Keithley 3402 Pulse Generator, a Hewlett-Packard 59307A VHF switchbox and an Agilent InfiniiVision MSO7104A oscilloscope. Some electrical measurements were performed in vacuum in a Janis ST-100-UHV-4 probe station equipped

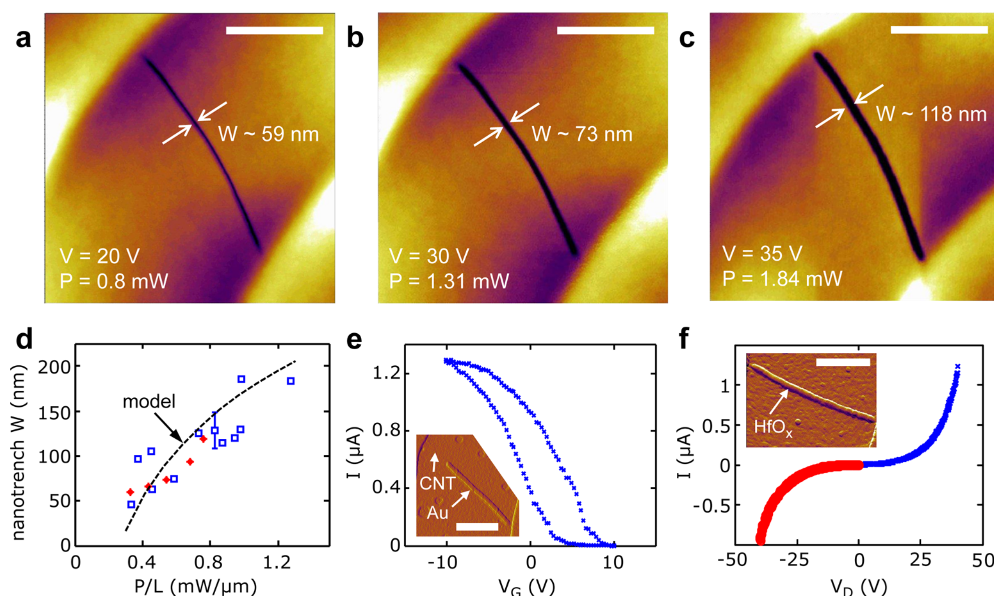

Figure 4. Tuning nanotrench formation and other applications. (a−c) AFM images of nanotrench formed in PMMA after the CNT is biased at different voltage and power for 5 s each, as listed on the panels. A metallic CNT was used with $L \sim 2.4$ μm and $d \sim 2.5$ nm. Nanotrenches were formed in vacuum and AFM imaged in air. The PMMA was removed and respun (~50 nm thick) after each step. Narrower trenches do not reach the Pd electrodes (at top-left and bottom-right of each image) due to cooling effect of metal contacts.[13] (d) Nanotrench widths scale approximately sublinearly with the input power per CNT length. Red stars are from the same device in panels a−c; blue squares are from other devices. The dashed curve is a computational model detailed in the Supporting Information. Error bar shows typical uncertainty in nanotrench width from the AFM measurement. Additional uncertainty (versus the model) is introduced by possible PMMA reflow during heating. (e,f) Electrical measurements and AFM images of two self-aligned NWs (~60 nm wide) with CNT electrodes enabled by this process. (e) Au NW aligned in series with semiconducting CNT, showing that gating of CNT (with bottom Si substrate, V_G) still controls current flow. (f) HfO_x NW aligned on metallic CNT nanogap. V_D is the voltage applied across the Pd electrodes of the CNT. All scale bars are 1 μm.

with a heating stage (up to 650 K). Threshold voltages (V_T) were determined from DC current sweeps with 40 V compliance. Reversible SET/RESET programming was performed with pulsed voltages. The pulse current amplitudes were calculated from the applied voltage and the known device resistance (*I*−*V* curves). The endurance measurements were automated via LabVIEW scripts. AFM measurements of CNT diameter,[33] length, and device topography were performed with an Asylum MFP-3D system. Most AFM measurements were done in air in tapping mode scan with a silicon tip of initial radius ~7 nm. The scan rate is typically 3−5 μm/s.

■ ASSOCIATED CONTENT

Ⓢ Supporting Information

Details of CNT device fabrication; PMMA film spin-coating, GST deposition and lift-off conditions; more AFM images of the self-aligned PCM nanowire devices; electrical characterization setup; additional data analysis; nanotrench formation process; finite element modeling; and applications of nanotube-nanowire self-aligned techniques. This material is available free of charge via the Internet at http://pubs.acs.org.

■ AUTHOR INFORMATION

Corresponding Author

*E-mail: epop@illinois.edu.

Present Address

⊥Korea Research Institute of Standards and Science, Daejeon 305−340, Korea.

Author Contributions

#Authors contributed equally.

Notes

The authors declare no competing financial interest.

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Supplementary Information

Self-Aligned Nanotube-Nanowire Phase Change Memory

Feng Xiong[1,2,3], Myung-Ho Bae[1,2,4,*], Yuan Dai[1,2,*], Albert D. Liao[1,2], Ashkan Behnam[1,2], Enrique A. Carrion[1,2], Sungduk Hong[1,2], Daniele Ielmini[5] and Eric Pop[1,2,3]

[1]*Micro & Nanotechnology Lab, University of Illinois, Urbana-Champaign, IL 61801, USA*

[2]*Dept. of Electrical & Computer Eng., University of Illinois, Urbana-Champaign, IL 61801, USA*

[3]*Beckman Institute, University of Illinois, Urbana-Champaign, IL 61801, USA*

[4]*Present address: Division of Convergence Technology, Korea Research Institute of Standards and Science, Daejeon 305-340, Korea*

[5]*Dipartimento di Elettronica e Informazione, Politecnico di Milano, 20133 Milano, Italy*

[*]Authors contributed equally.

Contact: epop@illinois.edu

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1. Fabrication of Carbon Nanotube Devices

Carbon nanotubes (CNTs) were grown by chemical vapor deposition (CVD) using a mixture of CH_4 and C_2H_4 as the carbon feedstock, and H_2 as the carrier gas at 900 ˚C[1]. Fe (~2 Å thick deposited by e-beam evaporation) is used as the catalyst for CNT growth. The catalyst was deposited on ~90 nm thick SiO_2 and highly p-doped Si wafers. Patterned catalyst islands are formed using photolithography and lift-off. Prior to growth, the catalyst was annealed at 900 ˚C in Ar environment to ensure the formation of Fe nanoparticles, from which the CNTs grow. The flow rate of CH_4 to C_2H_4 was large (~50:1) to grow predominantly single-walled CNTs or small-diameter (<5 nm) multi-wall CNTs. The nanotubes were contacted with Ti/Pd/Au (0.5/20/20 nm) electrodes defined using photolithography. An image of a typical CNT device is shown in Fig. 1a-b of the main text. The electrode separation on our test chips is varied from $L \approx$ 1-5 μm, although the exact CNT length is not essential for low-power GST switching, with the CNTs being much more conductive than the GST bit (~100 kΩ vs. 1 MΩ – 1 GΩ; also see main text Fig. 3)[2].

2. PMMA Coating, GST Deposition and Lift-Off

-PMMA Coating: After fabricating the CNT device, we spin a thin layer of poly(methyl methacrylate) (PMMA). The thin film thickness can be controlled by varying the spin rate and/or adding A-thinner into the PMMA 495 A2 solution. A thinner PMMA layer generates narrower nanotrenches upon Joule heating; while a thicker PMMA layer gives better lift-off results. The PMMA thickness was measured by ellipsometry and confirmed by AFM measurement. Table S1 shows the PMMA thickness under different conditions. Typical PMMA thickness used in this study is ~50 nm. The device is then baked at 200 ˚C for 90 seconds after spin coating.

-GST Deposition: In this work, $Ge_2Sb_2Te_5$ (GST) is deposited by dc sputtering with an AJA ATC 2000 custom four gun co-sputtering system. The GST sputtering target is of 99.999% purity, customer made from ACI Alloys Inc. Deposition power (6 W) and rate (0.1 Å/s) was kept minimal so as to minimize the damage to the PMMA thin film and to the CNT. This would ensure a smoother lift-off later on. Nevertheless, GST deposition by sputtering is found to cause some damage to semiconducting CNTs. By contrast, metallic CNTs appear to survive GST sputtering with little damage, most likely by virtue of being small-diameter multi-walled CNTs (i.e. it is possible that the outer wall protects the inner walls from sputtering damage). The GST thin film thickness is ~10 nm, confirmed by both X-ray reflectivity (XRR) and AFM measurements. Figure S2 depicts the XRR measurement results from a Philips Xpert Pro XRD system on a control sample (GST thin film on Si wafer).

Solution Composition	RPM	Thickness (nm)
50% PMMA, 50% A-thinner	4000	27
75% PMMA, 25% A-thinner	4000	40
100% PMMA	6000	45
100% PMMA	4500	52
100% PMMA	3500	57
100% PMMA	2500	86
100% PMMA	1500	113

Table S1 | PMMA Thickness. PMMA thickness under different spin rates and compositions.

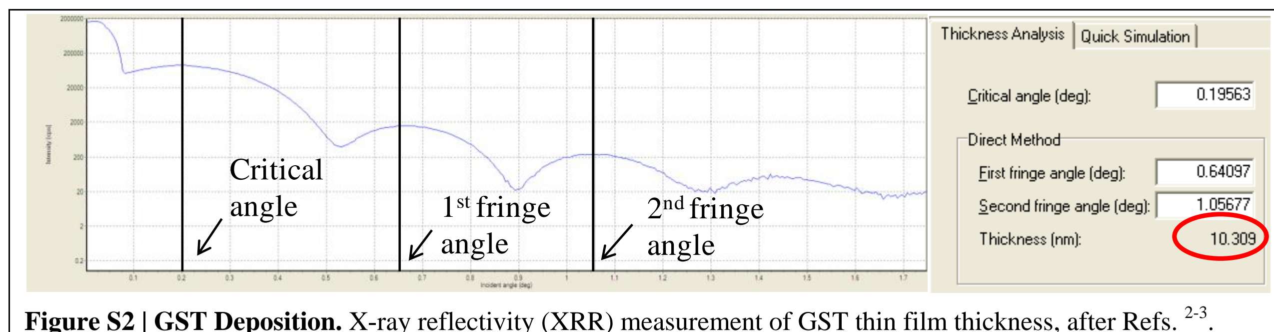

Figure S2 | GST Deposition. X-ray reflectivity (XRR) measurement of GST thin film thickness, after Refs. [2-3].

After GST deposition, we sometimes deposit a thin layer of encapsulation to prevent oxidation of GST when exposed to laboratory air. This capping layer also acts as a mechanical cap to suppress volume changes caused by phase change and improve device lifetime. We first tried sputtering 5 to 10 nm of SiO_2 or Al_2O_3 right after GST deposition without breaking the vacuum to obtain a clean interface between GST and the oxide cap. However, RF sputtering of either oxide would require relatively high power (> 100 W), which damages the PMMA film quality and often causes lift-off issues. Moreover, depositing the capping layer before lift-off would leave the sidewalls of the GST nanowire uncovered. Thus we chose to first perform lift-off to form the self-aligned GST nanowire; then we used e-beam evaporation to deposit ~10 nm of SiO_2 to cover up the entire sample. The e-beam evaporation was done in a Denton e-beam optical coater. Lift-off is performed by immersing the sample in warm acetone (50 to 60 ^{o}C) for 30 minutes. Sonicating the solution for 5 to 10 seconds improves lift-off results, though prolonged sonication is detrimental to the CNT device. In Fig. 1 (main manuscript) and Fig. S3 below, we show AFM measurements of a typical self-aligned nanotube-nanowire device at different stages.

3. Atomic Force Microscopy (AFM)

The AFM imaging was performed using a MFP3D™ Asylum AFM. Most scans were done in tapping mode with a silicon tip that has a nominal radius of 7 nm. The scan size was typically kept small, less than 5 µm × 5 µm with a scan rate of 1 Hz. The resolution was 512 × 512. The drive amplitude and set point were carefully monitored to ensure good tracking of the surface.

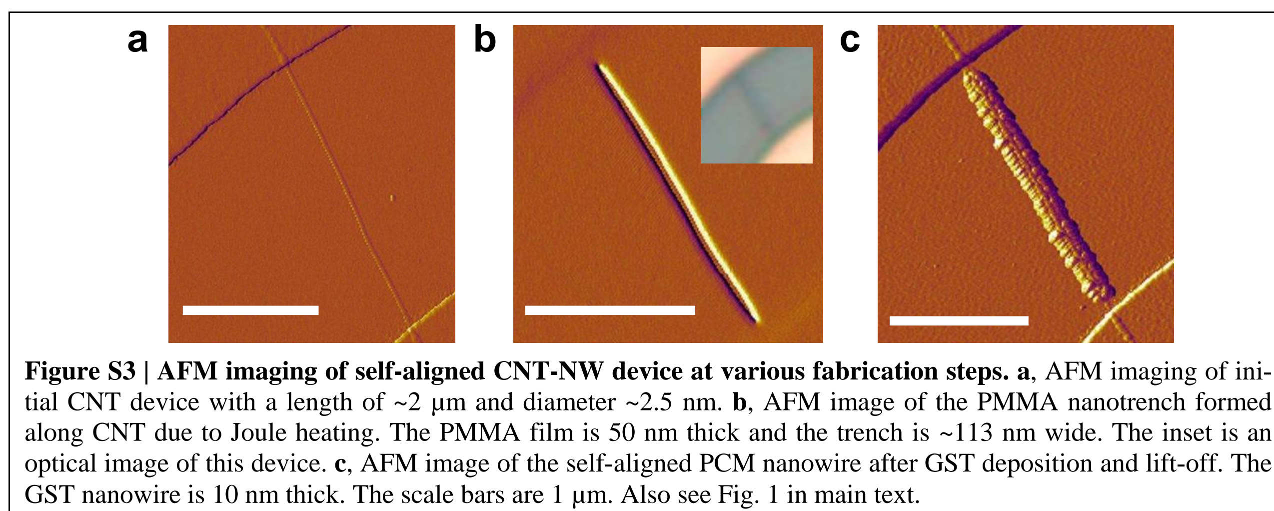

Figure S3 | AFM imaging of self-aligned CNT-NW device at various fabrication steps. a, AFM imaging of initial CNT device with a length of ~2 µm and diameter ~2.5 nm. **b**, AFM image of the PMMA nanotrench formed along CNT due to Joule heating. The PMMA film is 50 nm thick and the trench is ~113 nm wide. The inset is an optical image of this device. **c**, AFM image of the self-aligned PCM nanowire after GST deposition and lift-off. The GST nanowire is 10 nm thick. The scale bars are 1 µm. Also see Fig. 1 in main text.

4. Experimental Setup for Electrical Characterization

-DC measurements: All dc electrical characterizations were performed with a Keithley 4200 semiconductor characterization system (SCS). Some electrical measurements (e.g. PMMA nanotrench formation) were performed in vacuum (~10^{-5} torr) in a Janis ST-100-UHV-4 probe station equipped with a heating stage. Electrical breakdown of CNTs to form the nanogap was done in a probe station in air ambient, under an Ar flow nozzle[4]. During the dc SET operation of the PCM device (amorphous to crystalline or a → c transition), we monitored the voltage across the device while sweeping the current gradually. This prevents a sudden increase in current caused by large increase in device conductance during the phase change. The voltage compliance is set at 40 V during the current sweep. Note that SET transitions were created both with dc current sweeps (as outlined above and in Fig. 2b) and pulsed voltages (as outlined below).

-Pulsed measurements: We used a Keithley 3402 pulse generator to produce all the programming pulses. The SET pulse is typically 300-ns wide with 50-ns rising/falling edges; the RESET pulse is usually 50-ns in width with 2-ns edges. Shorter pulses, down to ~30-ns width have also been used to obtain lower programming energy per bit (see main text). However, the lower bound of our pulse capability is limited by our setup and specifically by the capacitance of the large contact pads to the CNT device. In principle, PCM switching even with ~1-ns pulse widths should be achievable as suggested by previous work[5-6]. This would reduce the operating energy in this work to the regime of single femtojoules per bit.

-Memory endurance test: Device endurance tests are automated via LabVIEW scripts. A typical cycle of the endurance test includes: 1) read the a-GST resistance at 0.5 V using Keithley 4200 SCS; 2) send a SET pulse for a → c phase transition using the pulse generator; 3) read the c-GST resistance at 0.5 V; 4) send a RESET pulse for c → a transition. A Hewlett-Packard 59307A VHF switchbox is used to switch the device connection between SCS and the pulse generator. Figure S4 shows the connections of a typical endurance test.

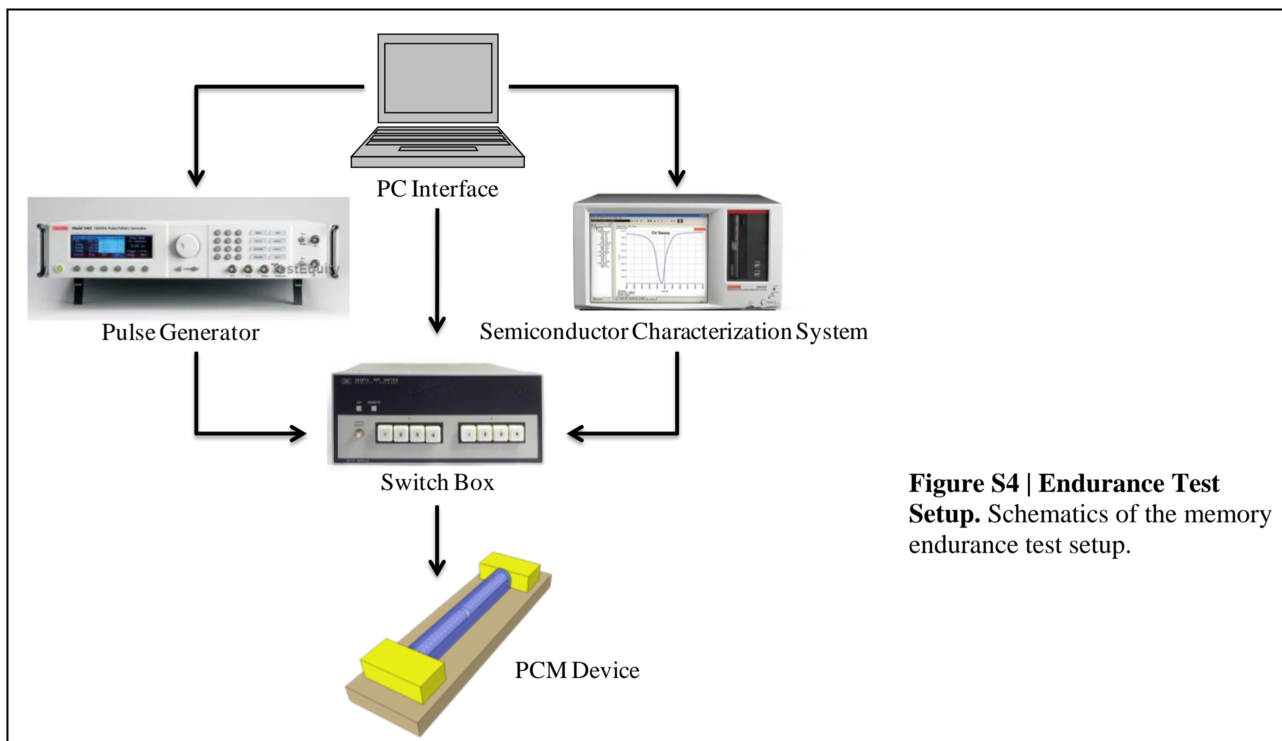

Figure S4 | Endurance Test Setup. Schematics of the memory endurance test setup.

5. More Data Analysis

-Self-aligned PCM nanotube-nanowire devices: A total of 102 self-aligned CNT-NW devices were tested in total. In addition to the characteristics shown in the main text, dc electrical and AFM measurements of other self-aligned PCM devices are shown in Fig. S5.

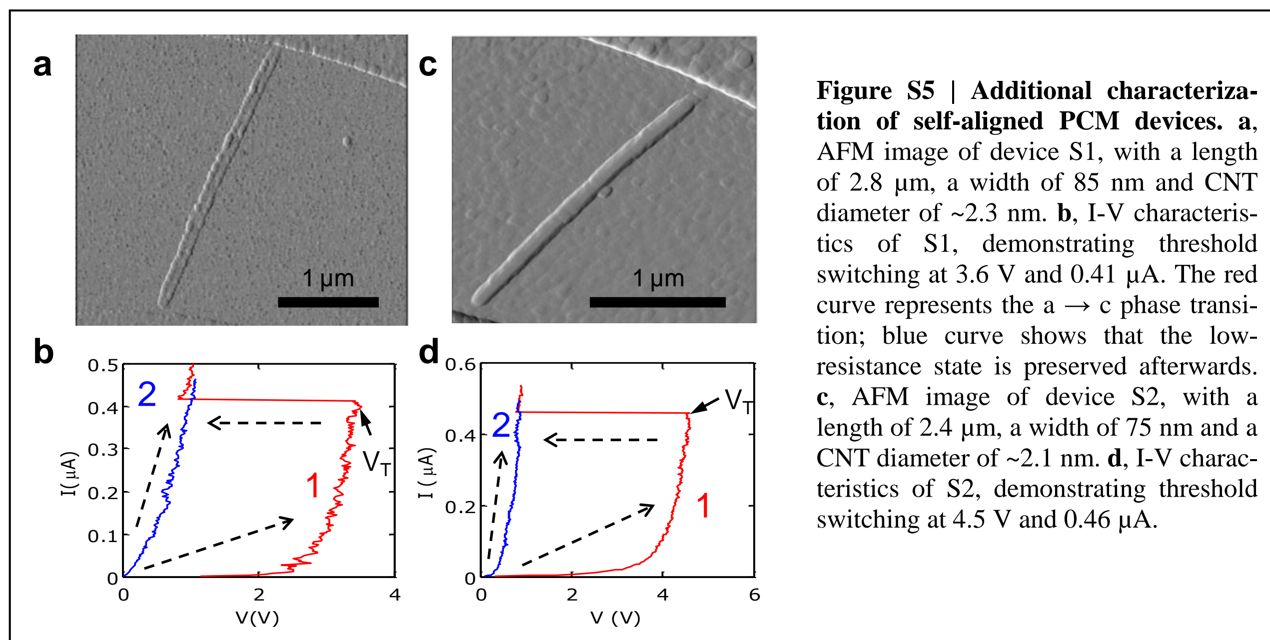

Figure S5 | Additional characterization of self-aligned PCM devices. a, AFM image of device S1, with a length of 2.8 µm, a width of 85 nm and CNT diameter of ~2.3 nm. **b**, I-V characteristics of S1, demonstrating threshold switching at 3.6 V and 0.41 µA. The red curve represents the a → c phase transition; blue curve shows that the low-resistance state is preserved afterwards. **c**, AFM image of device S2, with a length of 2.4 µm, a width of 75 nm and a CNT diameter of ~2.1 nm. **d**, I-V characteristics of S2, demonstrating threshold switching at 4.5 V and 0.46 µA.

-V_T reduction: As mentioned in the main text (Fig. 2b), the threshold voltage V_T of such devices typically decreases and stabilizes after a few programming cycles. This reduction in V_T is not uncommon, since the as-deposited amorphous material is different from the melt-quenched a-GST[7]. In Fig. S6a, we present a histogram of the initial V_T (bottom pane) and after several cycles of "burn-in" (top pane) for 24 devices. The V_T reduction ranges from 3.2% to as much as 40.3%, with an average of ~23%. In Fig. S6b, we see that the final V_T is ~77% of initial V_T.

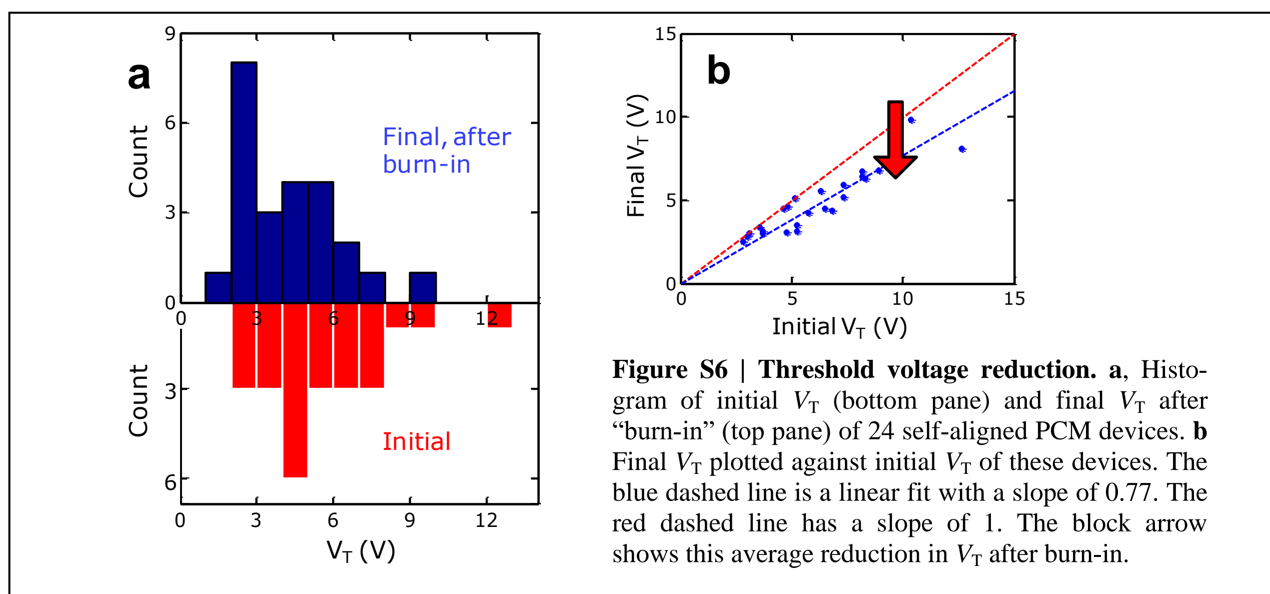

Figure S6 | Threshold voltage reduction. a, Histogram of initial V_T (bottom pane) and final V_T after "burn-in" (top pane) of 24 self-aligned PCM devices. **b** Final V_T plotted against initial V_T of these devices. The blue dashed line is a linear fit with a slope of 0.77. The red dashed line has a slope of 1. The block arrow shows this average reduction in V_T after burn-in.

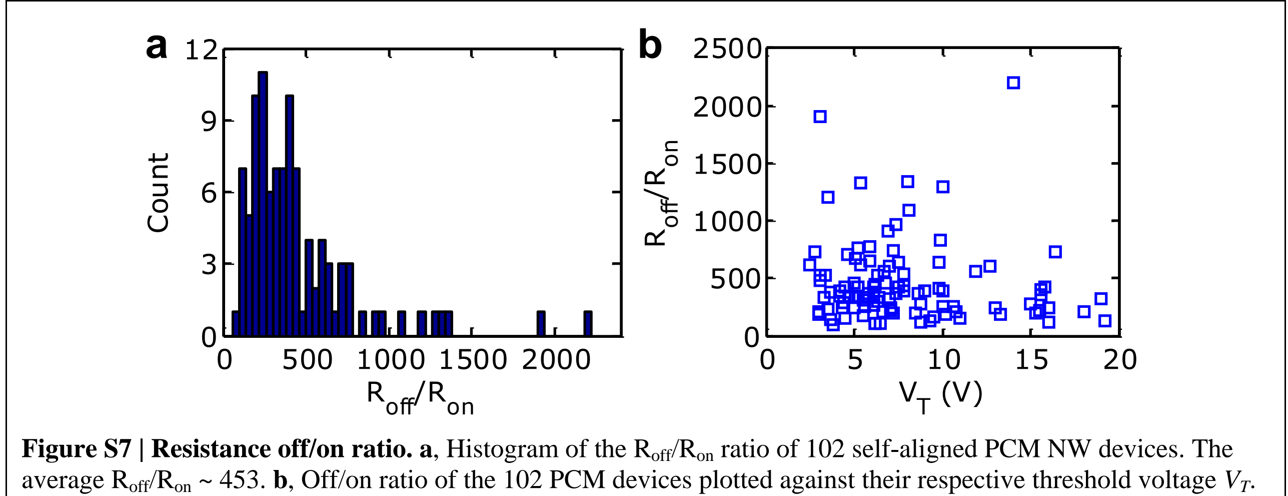

Figure S7 | Resistance off/on ratio. a, Histogram of the R_{off}/R_{on} ratio of 102 self-aligned PCM NW devices. The average R_{off}/R_{on} ~ 453. **b**, Off/on ratio of the 102 PCM devices plotted against their respective threshold voltage V_T.

-Resistance off/on ratio: Figure S7a shows the histogram of R_{off}/R_{on} for the 102 self-aligned PCM devices studied. The average R_{off}/R_{on} ~ 453 with the highest ratio ~2200. These values are >10× higher than previously reported in Ref. 3, due to the elimination of parallel leakage pathways. We also plotted the R_{off}/R_{on} against their respective threshold voltages in Fig. S7b.

-Device scaling analysis: We plot the threshold voltage V_T as a function of the initial CNT length in Fig. S8a and found a weak positive correlation. This is consistent with previous findings suggesting longer CNTs create larger nanogaps with our electrical breakdown method, which in turn results in higher threshold voltage[4, 8]. Longer CNTs also introduce slightly larger parasitic series resistance to the nanoscale PCM bit. Figure S8b plots the RESET current as a function of the GST nanowire width. There is no obvious trend in the plot. Coupled with findings shown in Fig. 3b in the main text, this suggests that the active bit phase change region is primarily determined by the CNT electrode size, and less so by the NW width[3].

-RESET current scaling: To see how this work compares to state-of-the-art PCM devices, Fig. S9a plots the RESET current against the CNT electrode contact area for our self-aligned de-

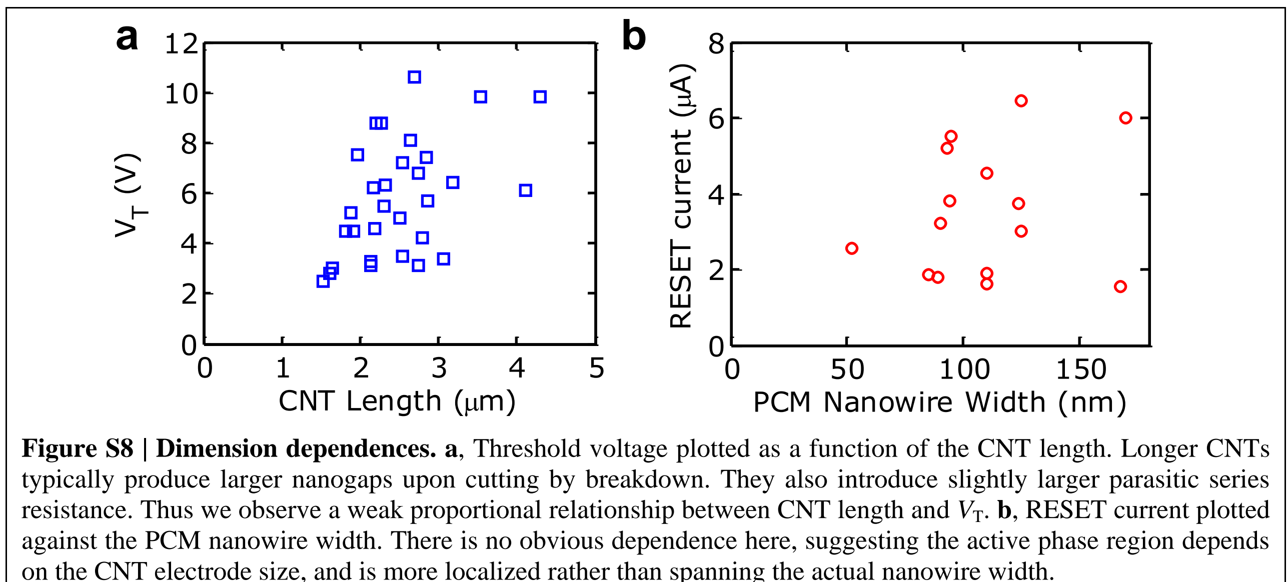

Figure S8 | Dimension dependences. a, Threshold voltage plotted as a function of the CNT length. Longer CNTs typically produce larger nanogaps upon cutting by breakdown. They also introduce slightly larger parasitic series resistance. Thus we observe a weak proportional relationship between CNT length and V_T. **b**, RESET current plotted against the PCM nanowire width. There is no obvious dependence here, suggesting the active phase region depends on the CNT electrode size, and is more localized rather than spanning the actual nanowire width.

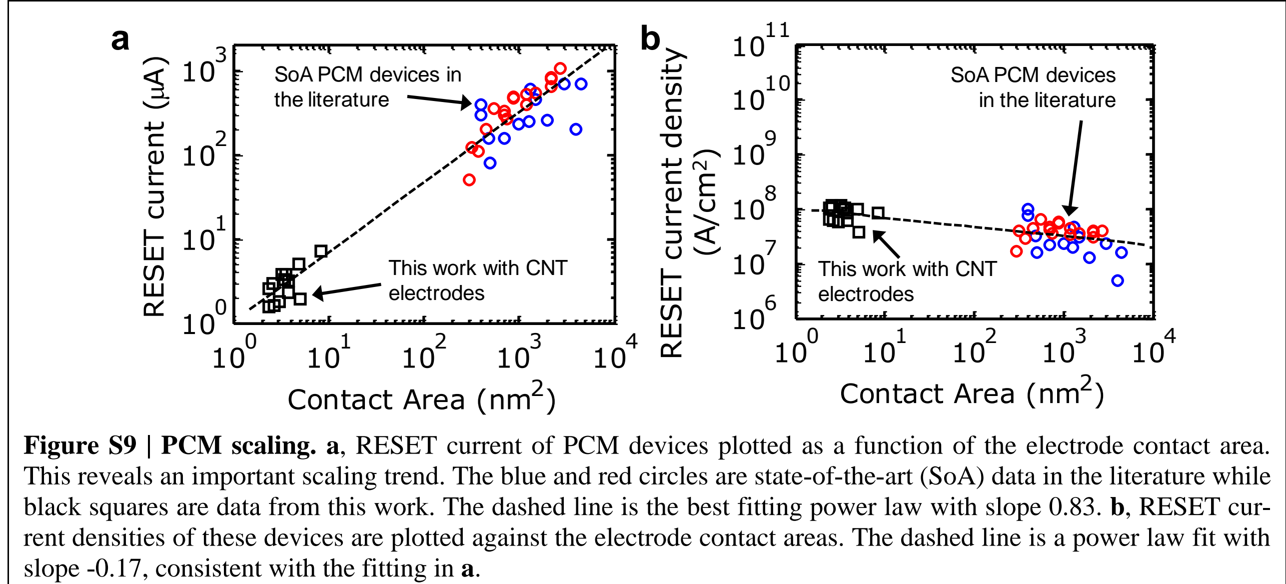

Figure S9 | PCM scaling. a, RESET current of PCM devices plotted as a function of the electrode contact area. This reveals an important scaling trend. The blue and red circles are state-of-the-art (SoA) data in the literature while black squares are data from this work. The dashed line is the best fitting power law with slope 0.83. **b**, RESET current densities of these devices are plotted against the electrode contact areas. The dashed line is a power law fit with slope -0.17, consistent with the fitting in **a**.

vices as well as other PCM devices reported in the literature[9-10]. We can see that our results fit with the general scaling trend observed, and scale approximately as ~$A^{0.83}$, where A is the contact area. This is expected for PCM devices that scale non-isotropically[11] (area and thickness are not scaled similarly), since the CNT diameter and the nanogap size do not correlate perfectly in our devices. The current densities of our PCM-NW devices and other PCM devices are plotted in Fig. S9b. The power fit (dashed line) has a slope of -0.17, consistently with Fig. S9a.

-Resistance drift: Figure S10 depicts drift behavior of two more self-aligned PCM nanotube-nanowire devices after RESET, with and without oxide capping layers. We observe the same trend as reported in the main text (Fig. 2f) and by others[12-13]. The resistance drift in the PCM nanowires is extremely low when uncapped. The drift coefficient for capped devices is slightly higher, but in line with previous measurements[9, 11-12].

-Activation energy: We also measured the activation energy of a-GST in our devices by measuring the subthreshold *I-V* characteristics at different temperatures (Fig. S11a). In Fig.

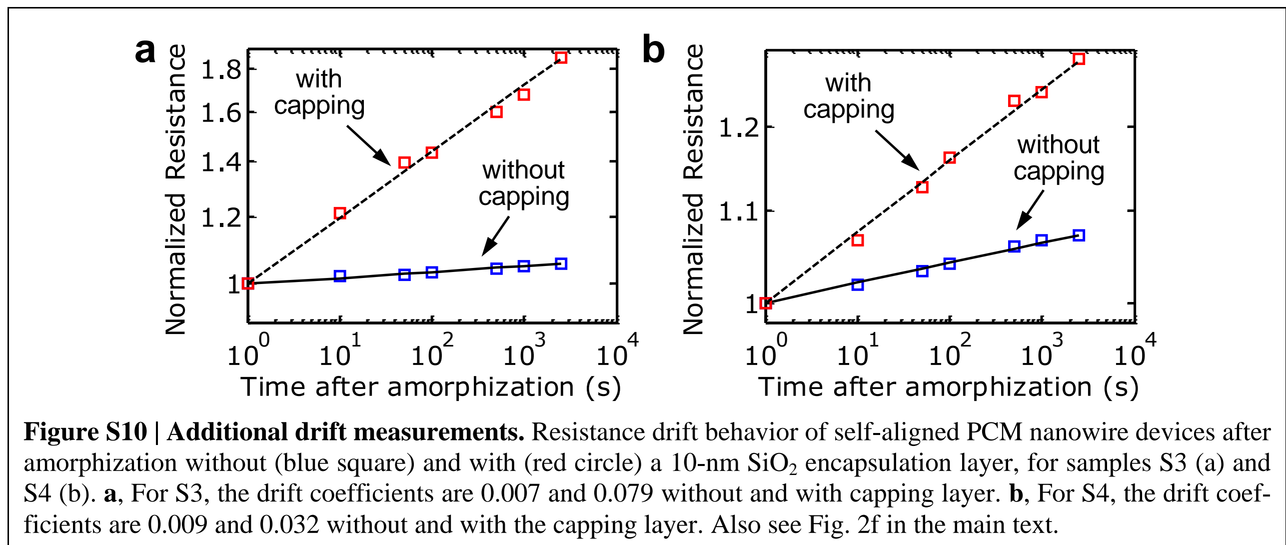

Figure S10 | Additional drift measurements. Resistance drift behavior of self-aligned PCM nanowire devices after amorphization without (blue square) and with (red circle) a 10-nm SiO_2 encapsulation layer, for samples S3 (a) and S4 (b). **a**, For S3, the drift coefficients are 0.007 and 0.079 without and with capping layer. **b**, For S4, the drift coefficients are 0.009 and 0.032 without and with the capping layer. Also see Fig. 2f in the main text.

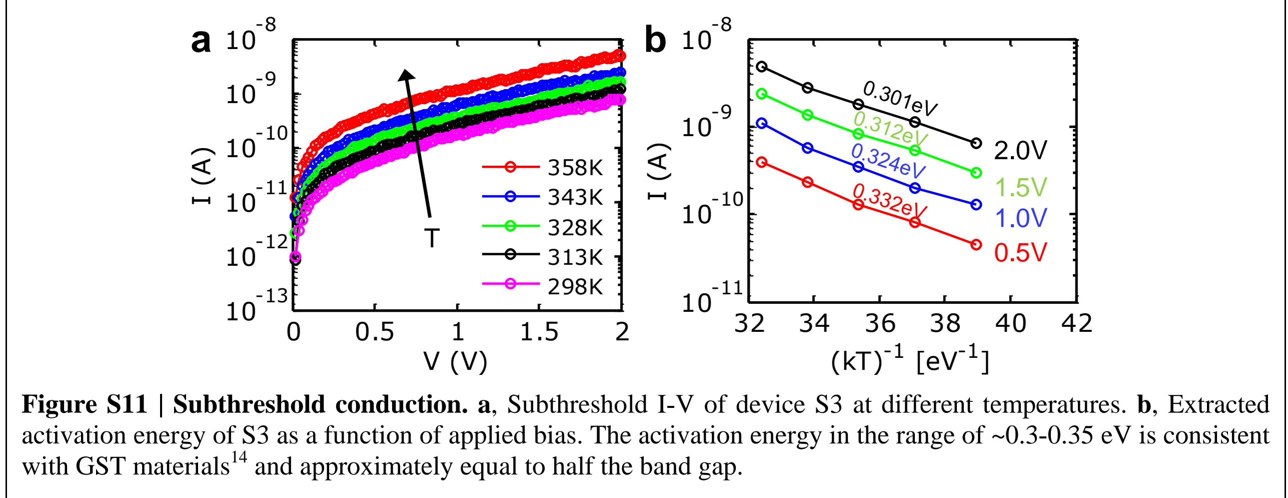

Figure S11 | Subthreshold conduction. a, Subthreshold I-V of device S3 at different temperatures. **b**, Extracted activation energy of S3 as a function of applied bias. The activation energy in the range of ~0.3-0.35 eV is consistent with GST materials[14] and approximately equal to half the band gap.

S11b, we can see that the activation energy of a-GST decreases as the applied bias increases, consistent with the Poole-Frenkel transport mechanism expected for amorphous chalcogenides[14].

-Device failure mode after cycling: The typical failure mode for our self-aligned PCM devices after cycling is the "stuck-reset" failure. In some cases, the device resistance enters into the high-resistance state after a reset pulse; and subsequent set pulses are not able to switch the device into the low-resistance anymore. We suspect these sudden failures are due to void formation and delamination in the PCM bit that irreversibly cut off the electrical pathway. In other cases, the device resistance remains low after the original reset pulse; applying a higher amplitude reset pulse can switch the device into the high-resistance state, at which point the device subsequently gets stuck, and it cannot be switched on by another set pulse. We attribute this behavior to possible crystalline halo formation around the nanogap, in devices where the NW constriction is not sufficiently narrow. And as we increase the reset voltage to try to re-amorphize the device, the catastrophic delamination/void formation process happens which severs the conduction path.

6. Nanotrench Formation

-Power dependence: The self-aligned nanofabrication process is not only a good approach to examine the fundamental scaling of PCM devices, but it also has the potential to be used as a platform for many other relevant applications. For instance, the nanotrench could be used to precisely position and measure other types of nanowires, nanoparticles, or even single molecules (such as DNA strands) between the two CNT electrodes. In order to extend the utility of this method, it is important to understand and control the nanotrench formation process. The nanotrench width depends on many parameters such as input power, bias duration, ambient temperature, PMMA thickness etc. Figure 4 in the main text already illustrates how the trench width varies with input power. In Fig. S12 below, we present additional AFM images of nanotrench formation under various power input conditions.

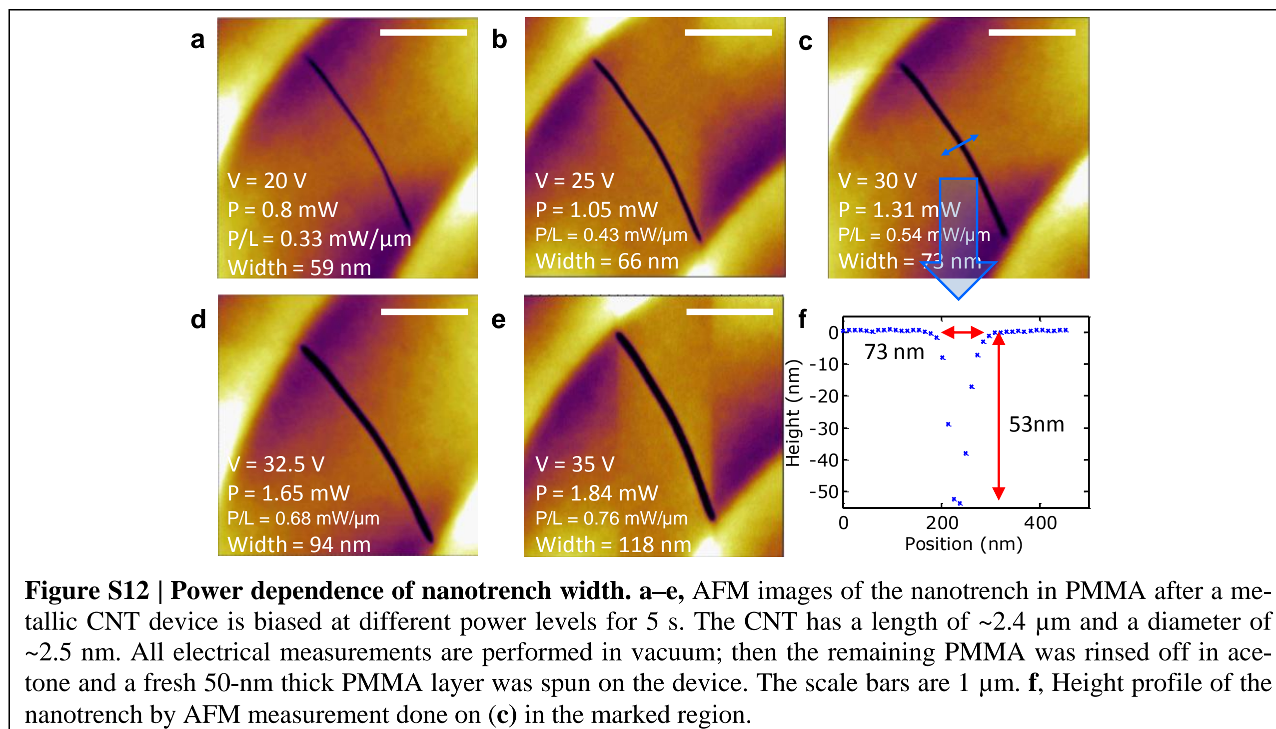

Figure S12 | Power dependence of nanotrench width. a–e, AFM images of the nanotrench in PMMA after a metallic CNT device is biased at different power levels for 5 s. The CNT has a length of ~2.4 µm and a diameter of ~2.5 nm. All electrical measurements are performed in vacuum; then the remaining PMMA was rinsed off in acetone and a fresh 50-nm thick PMMA layer was spun on the device. The scale bars are 1 µm. **f**, Height profile of the nanotrench by AFM measurement done on (**c**) in the marked region.

-Time dependence: We studied how the width of the nanotrench of a typical CNT device (Fig. S13a) covered by ~50 nm of PMMA changed as a function of the applied bias time, with everything else being constant. Figures S13b-d show the AFM images of the nanotrench of this device under 25 V dc bias for 1 s, 5 s and 10 s, respectively. The nanotrench width increases from 61 nm to 80 nm between 1 and 5 s, with no further increase beyond 5 s. This time scale is much longer than the thermal time constant of the system (a few hundreds of nanoseconds), suggesting that viscous flow plays a role in the trench formation process.

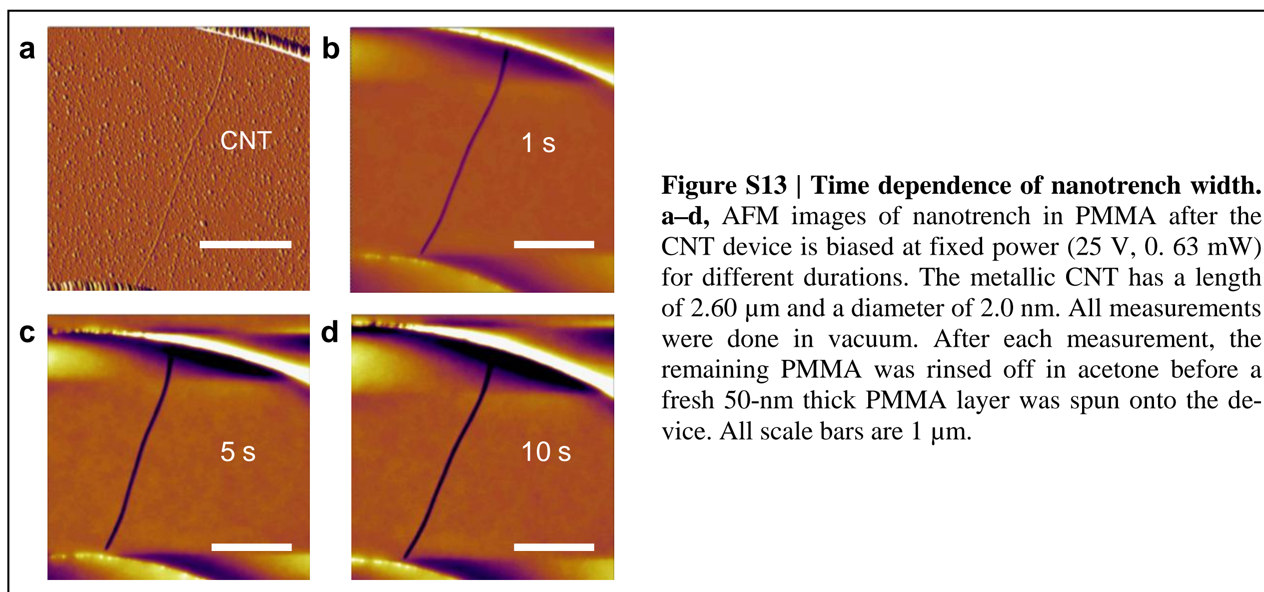

Figure S13 | Time dependence of nanotrench width. a–d, AFM images of nanotrench in PMMA after the CNT device is biased at fixed power (25 V, 0. 63 mW) for different durations. The metallic CNT has a length of 2.60 µm and a diameter of 2.0 nm. All measurements were done in vacuum. After each measurement, the remaining PMMA was rinsed off in acetone before a fresh 50-nm thick PMMA layer was spun onto the device. All scale bars are 1 µm.

7. Finite Element Modeling

-Simulation model: We developed a finite element model using COMSOL Multiphysics to numerically evaluate the temperature profile in PMMA during nanotrench formation. This also serves as the simulation platform that could guide us in optimizing the nanotrench formation process in the future. The schematics of this 3-dimensional model are shown in Fig. S14. In order to save simulation resources and time, we assumed that the device is perfectly symmetric and only simulated one quadrant. The planes of symmetry are along the CNT axis and the plane perpendicular to the CNT. The CNT diameter is 2 nm with a total length of 2 μm, on top of 90-nm thick SiO_2 (area = 50 μm × 5 μm). The bottom Si layer is 100 μm thick. The PMMA thin film is on top of the oxide layer and is typically 50 nm thick, unless otherwise specified.

The thermal conductivities of the CNT, SiO_2, Si and PMMA are 3300, 1.4, 150 and 0.2 W/(m·K), respectively[15]. Thermal boundary resistances[16] are simulated at all interfaces and have typical values ranging from 0.5 – 1 × 10^8 W/(m^2·K). Convection cooling and radiation loss can be ignored in this model. Thus, most external boundary conditions are set as adiabatic, except at the bottom and sidewall, where the temperature is set as the constant ambient temperature.

-Simulation results: The PMMA boiling point is assumed to be T_b ~ 260 ˚C. The nanotrench width is calculated by plotting the temperature contour in PMMA, as in Fig. 4d of the main text. Figure S14c summarizes the simulation results at different temperatures (200-400 K) and different input power. These results show an approximately sub-linear scaling trend, and suggest that we could create sub-20 nm trenches at low ambient temperatures and lower input power. These possibilities will be investigated in more details in the future.

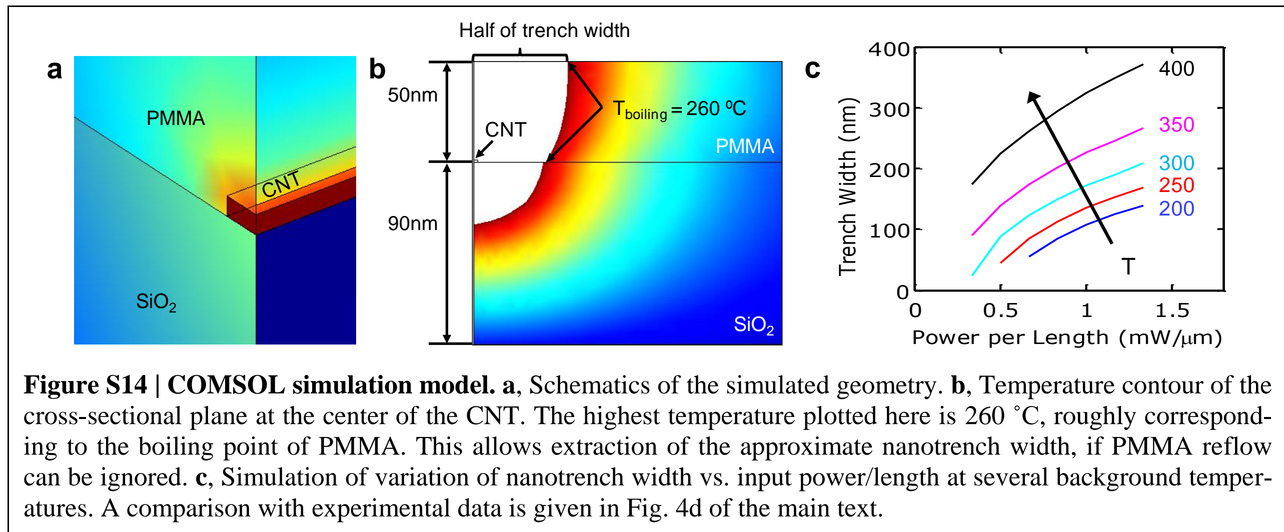

Figure S14 | COMSOL simulation model. a, Schematics of the simulated geometry. **b**, Temperature contour of the cross-sectional plane at the center of the CNT. The highest temperature plotted here is 260 ˚C, roughly corresponding to the boiling point of PMMA. This allows extraction of the approximate nanotrench width, if PMMA reflow can be ignored. **c**, Simulation of variation of nanotrench width vs. input power/length at several background temperatures. A comparison with experimental data is given in Fig. 4d of the main text.

8. Applications to Metal Nanowire and Resistive Random Access Memory (RRAM)

-Metal nanotube-nanowire devices: Other than PCM device scaling, we have also explored other applications of this self-aligned fabrication technique. Figure S15 shows results for self-aligned Au NWs deposited into the nanotrench along a CNT. Due to the contact cooling effect, there exists a thermal healing length along the CNT near the contacts where the temperature is low[17]. This is evident in some AFM images, when the nanotrench does not form all the way to

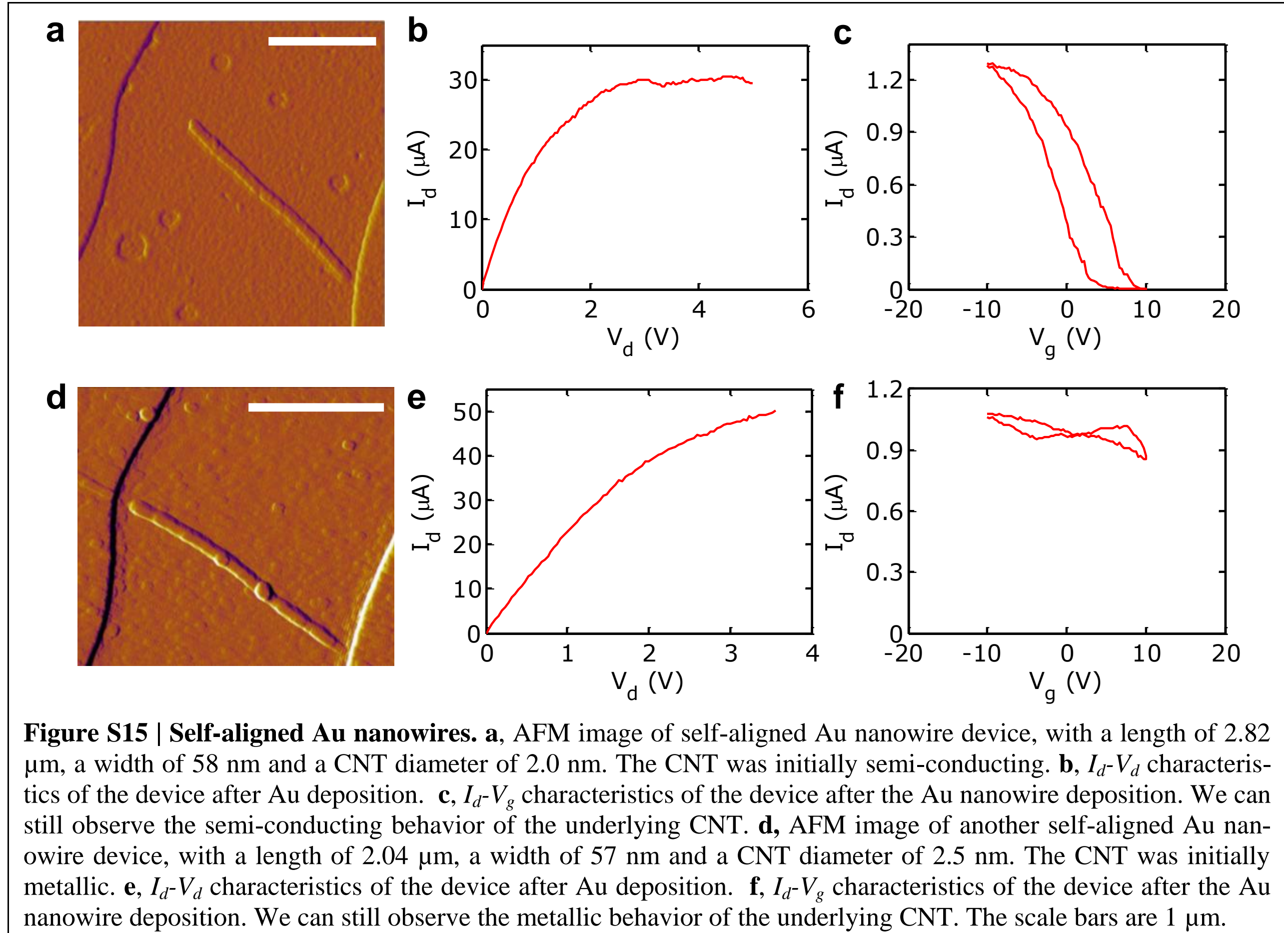

Figure S15 | Self-aligned Au nanowires. a, AFM image of self-aligned Au nanowire device, with a length of 2.82 μm, a width of 58 nm and a CNT diameter of 2.0 nm. The CNT was initially semi-conducting. **b**, I_d-V_d characteristics of the device after Au deposition. **c**, I_d-V_g characteristics of the device after the Au nanowire deposition. We can still observe the semi-conducting behavior of the underlying CNT. **d,** AFM image of another self-aligned Au nanowire device, with a length of 2.04 μm, a width of 57 nm and a CNT diameter of 2.5 nm. The CNT was initially metallic. **e**, I_d-V_d characteristics of the device after Au deposition. **f**, I_d-V_g characteristics of the device after the Au nanowire deposition. We can still observe the metallic behavior of the underlying CNT. The scale bars are 1 μm.

the metal contact, and no Au can be deposited. Thus, by creating the nanotrench in PMMA via local Joule heating and then evaporating Au into the trench, we could fabricate a much shorter CNT device with length in the hundreds and even tens of nanometer regime, as shown in Fig. S15a (here for a semiconducting CNT). Thus, in Fig. S15a-c we created a "short" Au nanowire in series with a "short" semiconducting CNT, whereas in Fig. S15d-e we created a "long" Au nanowire positioned along a metallic CNT. Device *I-V* curves in Fig. S15 suggest that semiconducting or metallic CNTs retain their original chirality after Au nanowire deposition.

-RRAM nanotube-nanowire devices: TiO_x and HfO_x are other materials as switching elements for future resistive random access memory (RRAM)[18-19]. We used our self-aligned process to fabricate RRAM nanotube-nanowire devices. In Fig. S16, we show AFM images of self-aligned TiO_x and HfO_x nanowires with CNT electrodes. Both oxides were 10 nm thick and e-beam evaporated. A non-Ohmic I-V characteristic, with a decrease of resistance at high voltage, is observed in both cases. The small hysteresis in the I-V curve of TiO_x under positive bias reveals a resistive-switching effect, while no hysteretic behaviors were seen in HfO_x. This might be due to the CNT nanogaps (typically ~50 nm) being too large for RRAM applications, as well as unoptimized metal-oxide composition.

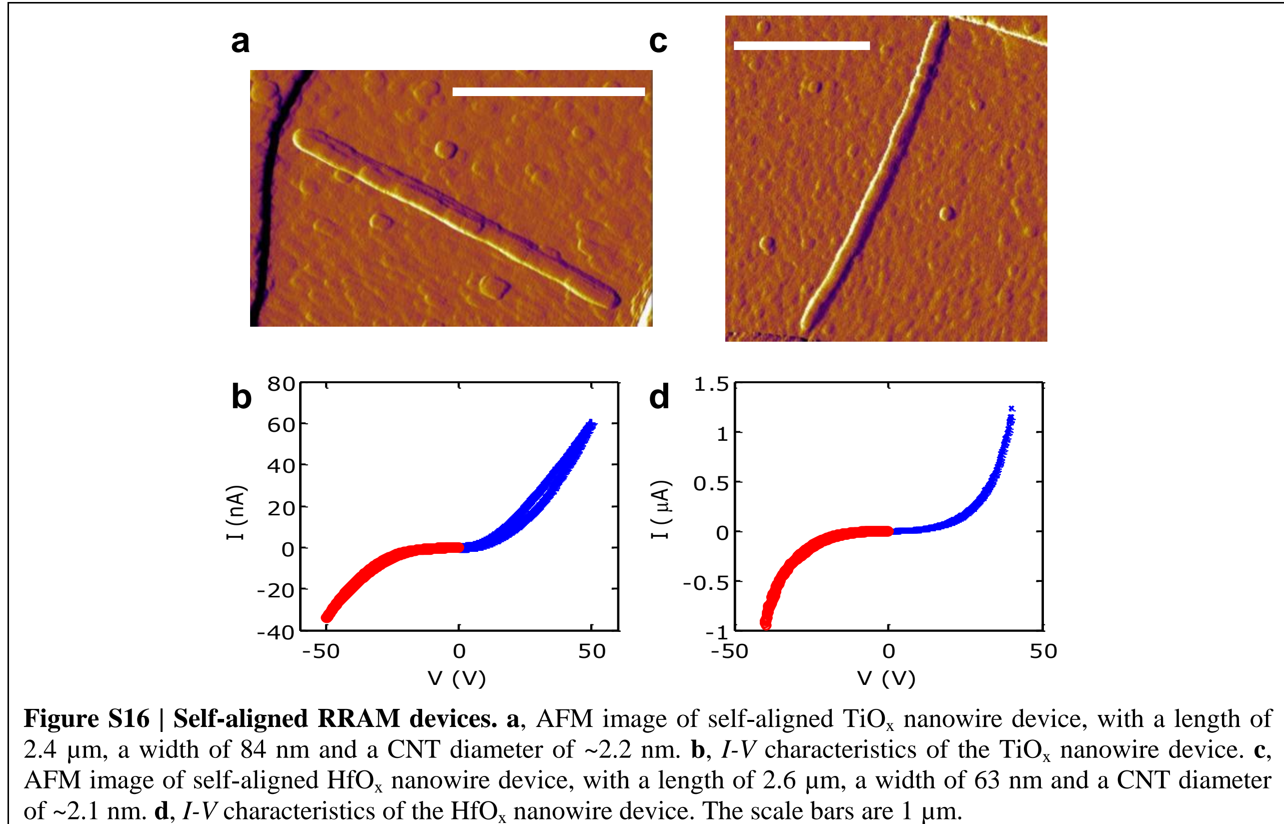

Figure S16 | Self-aligned RRAM devices. a, AFM image of self-aligned TiO_x nanowire device, with a length of 2.4 µm, a width of 84 nm and a CNT diameter of ~2.2 nm. **b**, *I-V* characteristics of the TiO_x nanowire device. **c**, AFM image of self-aligned HfO_x nanowire device, with a length of 2.6 µm, a width of 63 nm and a CNT diameter of ~2.1 nm. **d**, *I-V* characteristics of the HfO_x nanowire device. The scale bars are 1 µm.

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