THERMAL PHENOMENA IN NANOSCALE TRANSISTORS

Eric Pop[1] and Kenneth E. Goodson[2]
Dept. of [1]Electrical and [2]Mechanical Engineering, Stanford University
Stanford, CA 94305. E-mail: goodson@stanford.edu

ABSTRACT

As transistor gate lengths are scaled to 50 nm and below thermal device design is becoming an important part of microprocessor engineering. Decreasing dimensions lead to nanometer-scale hot spots in the transistor drain region, which may increase the drain series and source injection electrical resistances. Such trends are accelerated with the introduction of novel materials and non-traditional transistor geometries, like ultra-thin body, FinFET, or nanowire devices, which impede heat conduction. Thermal analysis is complicated by sub-continuum phenomena including ballistic electron transport, which displaces and reshapes the hot spot region compared with classical diffusion theory predictions. Ballistic phonon transport from the hot spot and between material boundaries impedes conduction cooling. The increased surface to volume ratio of novel transistor designs also leads to a larger contribution from material boundary thermal resistance. This paper surveys trends in transistor geometries and materials, along with their implications for the thermal design of electronic systems.

INTRODUCTION

The technological revolution that started with the introduction of the transistor just over half a century ago is without parallel in the way it has shaped our economy and our daily lives. The current trend toward nanoscale electronics is expected to have a similar impact into the third millennium. Commercial microprocessors are already available with transistors whose smallest lateral feature size is less than 100 nm and the thinnest material films are below 2 nm, or only a few atomic layers thick. Such miniaturization has led to tremendous integration levels, with a hundred million transistors assembled together on a chip area no larger than a few square centimeters. Integration levels are projected to reach the gigascale as the smallest lateral device feature sizes approach 10 nm. The most often cited technological roadblock of this scaling trend is the "power problem," i.e. power densities, heat generation and chip temperatures reaching levels that will prevent the circuits' reliable operation. Chip-level power densities are currently on the order of 100 W/cm^2, and if the rates of integration and miniaturization continue to follow the ITRS guidelines [1], the chip-level power density is likely to increase even further [2]. Higher power densities will quickly drain batteries out of portable devices and render most advanced, future electronics unusable without significant cooling technology, or fundamental shifts in design. The situation is compounded by millimeter-scale hot spots on the chip, i.e. localized regions of higher heat generation rate per unit area, hence higher temperatures (e.g. near the clock).

While the total heating rate of microprocessor chips has received much attention, a different thermal management challenge faces device and circuit designers at nanometer length scales, within individual transistors. Novel, complicated device geometries tend to make heat removal more difficult, and most new materials being introduced in device processing have lower thermal conductivities than bulk silicon (Fig. 1 and Table 1). In addition, sub-continuum effects must be taken into account in the thermal modeling of devices with dimensions less than the electron or phonon mean free path. These include ballistic electron and phonon transport, which lead to nanometer-sized hot spots in the device drain region. The non-local transport conditions cause such hot spots to be spatially displaced and have a higher temperature rise compared with classical heat diffusion theory predictions. Also, the thermal conductivity of semiconductor films thinner than the phonon mean free path is significantly reduced by phonon confinement and boundary scattering.

This manuscript reviews the thermal management issues associated with nanometer-scale transistors. The first section introduces a novel method for computing heat (phonon)

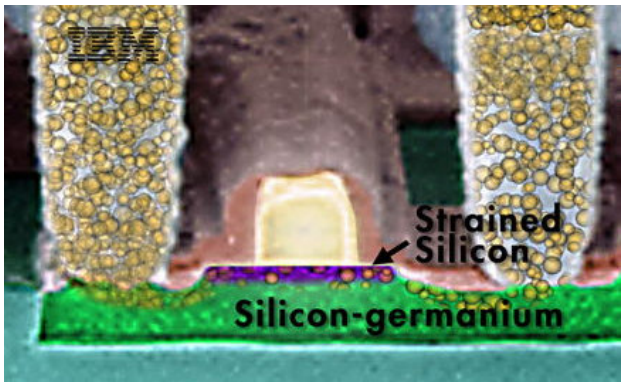

Fig. 1: False-color Transmission Electron Microscopy (TEM) cross-section of a future-generation strained silicon-on-insulator (SSOI) transistor. Image courtesy IBM.

generation rates in semiconductors, with the aid of Monte Carlo simulations. The next section discussed the impact of various material choices on the heat transport characteristics of future-generation transistors. The remainder of the paper is dedicated to an overview of heat transfer issues in four types of semiconductor transistors (bulk silicon, thin film devices, germanium devices and nanowires), with particular emphasis on the sub-continuum aspects of their behavior.

HEAT GENERATION

Modern device technologies already operate at length scales on the order of the electron and phonon mean free paths (approximately 5-10 and 200-300 nm in bulk silicon at room temperature, respectively [5][6]), and future technologies are going to forge deeper into this sub-continuum regime. Ballistic conditions will soon dominate both electron (current) and phonon (heat) transport, leading to strong non-equilibrium between the energy carriers at nanometer length scales. The electron-phonon interaction is neither energetically nor spatially uniform and the generated phonons have widely varying contributions to heat transport: optical phonons make virtually no contribution to the thermal conductivity, which is dominated by longitudinal acoustic phonon transport [6].

In the context of a transistor, the applied voltage leads to a lateral electric field which peaks near the device drain (Fig. 4). This field accelerates the free charge carriers (e.g. conduction band electrons in a n-MOSFET) which gain energy, therefore "heating up." Electrons can scatter with each other, with lattice vibrations (phonons), interfaces, imperfections or impurity atoms. Of these, electrons only lose energy by scattering with phonons, consequently heating up the lattice (i.e. Joule heating). Other scattering mechanisms only affect the electron momentum [5]. The lattice absorbs the extra electron energy, heats up, and in turn affects the electronic transport properties of the material: the electron mobility in bulk silicon decreases approximately as $T^{-2.4}$ around room temperature.

In silicon, as in most semiconductors, high field Joule heating is typically dominated by optical phonon emission. Optical phonons are slow and they make virtually no contribution to heat transport. Rather, they decay into the faster acoustic modes, which carry the energy away from the hottest regions. Optical to acoustic decay times are relatively long (on the order of picoseconds [7]) compared to the electron-phonon scattering time (tenths of picoseconds). If the generation rate of optical modes due to Joule heating from current flow is higher than their rate of decay into acoustic modes, a phonon energy bottleneck is created and the optical mode density can build up over time, directly affecting electron transport.

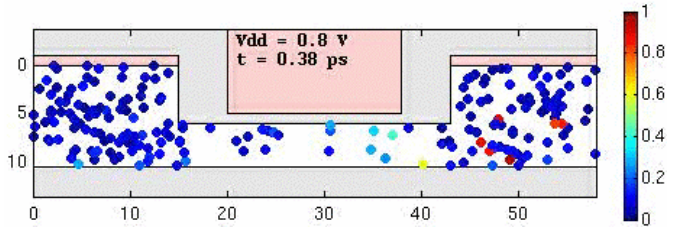

Fig. 3: Snapshot of electron transport in a future-generation thin-body silicon-on-insulator (SOI) device simulated with the Monte Carlo code MONET [10][12]. The color scale is the electron energy in eV and the device dimensions are in nm.

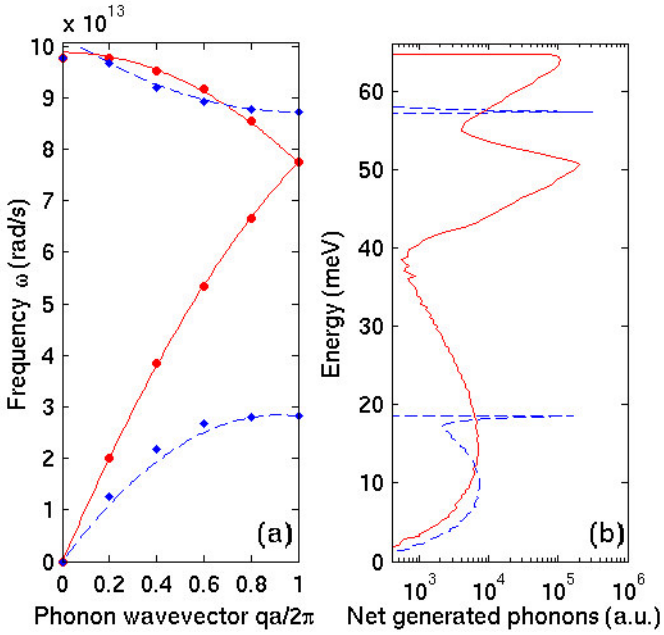

Fig. 2: Phonon dispersion in the (100) direction of silicon (a) and computed net (emission minus absorption) phonons generated by Joule heating (b). The symbols in (a) are from neutron scattering data [15] and the lines are a quadratic fit [10]. Solid lines are for longitudinal, and dashed lines are for transverse phonons. Optical modes are above and acoustic modes have energies below approximately 51 meV, respectively. Note the vertical axes are matched to facilitate comparison of the dispersion and generated modes.

The volumetric Joule heating rate can be simulated as the dot product of the electric field (**E**) and current density (**J**) [7]. Unfortunately, this approach does not account for the *microscopic* non-locality of the phonon emission near a strongly peaked electric field region, such as the drain of a transistor. Although electrons gain most of their energy at the location of the electric field peak, they typically travel another mean free path before releasing this energy to the lattice, in decrements of (at most) the optical phonon energy. The entire energy gained by electrons while traveling through the high field region is released over several mean free paths. Assuming an electron velocity of 10^7 cm/s (the saturation velocity in silicon) and an electron-phonon scattering time around 0.05 ps for the high-field region, the electron-phonon mean free path is about 5 nm. While such a small discrepancy may be neglected on length scales of microns, or even tenths

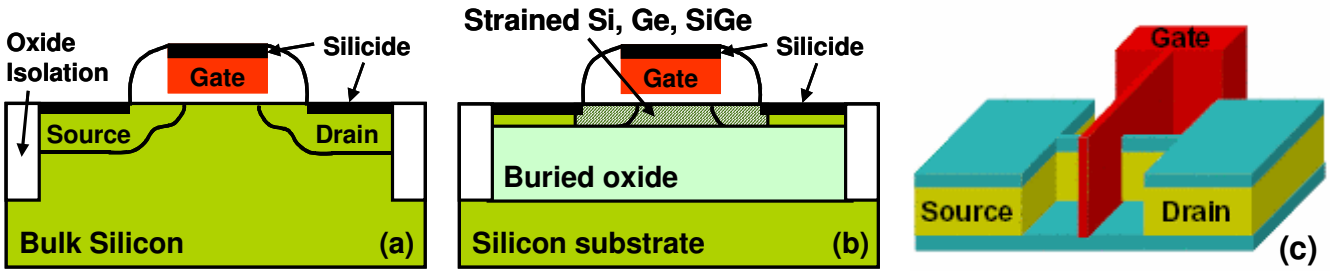

Fig. 4: Evolution of transistor designs from the bulk silicon "workhorse" (a) to (strained) silicon or germanium on insulator (b), to dual-gate or FinFET devices (c). Non-traditional device designs like (b) and (c) introduce more complicated geometries and lower thermal conductivity materials, making heat removal more difficult. The gate length (currently just under 100 nm) is expected to be scaled to the ten nanometer range, while the semiconductor film and "fin" thickness of (b) and (c) respectively, are approximately one quarter to one half the gate length. Figure (c) is from the technology roadmap (ITRS) [1].

of a micron, it must be taken into account when simulating heat generation rates on length scales of 10 nm, as in a future generation transistor. This leads to the formation of a nanometer-sized hot spot in the drain region of a transistor that is spatially displaced (by several mean free paths) from continuum theory predictions. In addition, the $\mathbf{J}\cdot\mathbf{E}$ formulation of the Joule heating also does not differentiate between electron energy exchange with the various phonon modes, and does not give any spectral information regarding the types of phonons emitted.

A Monte Carlo (MC) simulation method was recently introduced to compute sub-continuum and phonon mode-specific heat generation rates, with applications at nanometer length scales [10][11]. Both the electron energy bands and the phonon dispersion can be modeled analytically as ellipsoids and quadratics, respectively. This is a good approximation for devices operating at voltages below the silicon band gap (1.1 V), such as those of future technologies, and it enables significantly faster code that is easier to implement and debug. Impact ionization is suppressed at sub-band gap voltages, so it can be safely ignored. Inelastic scattering with all six known inter-valley, as well as intra-valley phonons was incorporated. Particular care was taken to treat the acoustic phonon interaction inelastically, including the phonon dispersion. An isotropic, analytic fit to the dispersion relation (see Fig. 2a) was also used to compute the final state after scattering with both optical and acoustic phonons, satisfying momentum and energy conservation.

The phonon emission and absorption events during a simulation run are tallied and full heat generation statistics can be collected. Fig. 2b shows the net (emission minus absorption) generated phonons during a typical simulation of current flow and Joule heating in a silicon resistor with a constant 50 kV/cm applied electric field. The shape of the generated phonon distribution approximately follows the density of states, while the specific phonons involved are given by the various scattering selection rules [14]. The area under each peak is proportional to the square of the coupling constant (deformation potential) of the respective electron-phonon interaction, and is a measure of the strength of each scattering type [9][10]. The broadening of the phonon generation peaks occurs when energetic electrons, farther away from the conduction band minima in the Brillouin zone, are allowed to scatter with phonons outside those strictly dictated by the geometrical selection rules. This is a direct consequence of using a continuous analytic representation of the phonon dispersion in selecting the final states. The resulting phonon generation spectra can be used as inputs for molecular dynamics or phonon Monte Carlo simulators [15], and they offer a comprehensive look at the complexity of Joule heating in silicon. The code can also be run in the context of a realistic device design, collecting electron transport and heat generation information across the simulation domain (Fig. 3).

Similar heat generation statistics could also be evaluated for different materials (e.g. germanium) as well as for strained or confined nanostructures. Restricted dimensions may lead to confined phonon modes [17], but the electron-phonon scattering rate can be recomputed taking into account the modified phonon dispersion. This can be done efficiently as long as the phonon dispersion is recast as a set of analytic functions (e.g. polynomials). More information on this Monte Carlo tool (named MONET) can be currently found online [12] and the code will be made available through the NCN/Purdue Computational Nanohub [13].

MATERIAL THERMAL PROPERTIES

Traditional, bulk transistor designs (Fig. 4a) typically incorporate only a few materials, most notably silicon, silicon dioxide insulators and silicided (e.g. NiSi) contacts. The high thermal conductivity of bulk silicon (148 $Wm^{-1}K^{-1}$) facilitates heat transport from the transistor channel down to the backside of the chip, where it has been traditionally removed with a heat sink.

Advanced, non-traditional device fabrication introduces a number of new materials with lower thermal conductivities. The thermal properties of these materials are therefore expected to play a more significant role in device design and

Table 1: Thermal conductivities of a few materials used in semiconductor device fabrication. Phonon boundary scattering significantly reduces the thermal conductivity of a 10 nm thin silicon film.

Material	Thermal Conductivity ($Wm^{-1}K^{-1}$)
Si	148
Ge	60
Silicides	40
Si (10 nm)	13
SiO_2	1.4

thermal behavior. Table 1 lists the thermal conductivities of a few materials used in semiconductor device fabrication. Bulk germanium transistors, for example, would suffer from increased operating temperatures due to a substrate thermal conductivity approximately 60 percent lower than bulk silicon transistors. Strained silicon channel devices (Fig. 4b) grown on a graded $Si_{1-x}Ge_x$ buffer layer benefit from an increased mobility due to band degeneracy splitting and a lighter effective mass in the strained film. However, their thermal behavior is adversely affected by the lower thermal conductivity of the $Si_{1-x}Ge_x$ alloy layer. The situation is worse for thin body devices grown on a silicon dioxide film. From an electrical point of view, silicon-on-insulator (SOI) devices benefit from lower capacitive coupling with the substrate, and hence increased switching speeds. Thermally, however, they are significantly affected by the very low thermal conductivity of the buried oxide layer, which is about two orders of magnitude less than that of silicon. The thermal conductivity of thin semiconductor films (thinner than the phonon mean free path) is also significantly reduced by phonon boundary scattering. A 10 nm thin silicon film is expected to have a thermal conductivity reduced by an order of magnitude from that of bulk silicon, based on theoretical estimates [4]. Although experimental data for such thin films does not yet exist, this estimate is based on extrapolations to available data [6], and also supported by recently measured reduced thermal conductivities in silicon nanowires [18].

The small dimensions of future device designs also imply a large surface-to-volume ratio (Fig. 4), and hence a stronger effect of material boundary resistance. Very few estimates exist on the magnitude of the *thermal* boundary resistance between dissimilar materials (e.g. a dielectric and a metal). Some measurements indicate it is on the order of the thermal resistance of a 20 nm thick silicon dioxide film [21], and fairly independent of processing conditions or the specific type of metal and dielectric involved. This is a significant value for nanoscale devices, and very important to understand. As more materials (e.g. high-k dielectrics, germanium, various silicides) are introduced in semiconductor processing, there is a growing need to understand the magnitude of boundary thermal resistance and its significance in future nanoscale device behavior. The boundary thermal resistance plays a significant role, for example, when a metal electrode is placed on top of the high-k gate dielectric (as expected for threshold voltage control in future technologies) as well as for device metal contacts and interconnects. More measurements are needed in this area, while more available data on thermal boundary resistance would also help toward a better understanding (and modeling) of the atomic scale interaction at the interface between two materials.

BULK SILICON TRANSISTORS

The bulk CMOS silicon transistor (Fig. 4a) has been (and still is) the principal building block of the semiconductor industry for the past 40 years. Thermal transport in bulk transistors has traditionally been modeled in the classical limit, as sub-continuum effects could be neglected for device dimensions larger than the phonon mean free path. As devices are scaled below 100 nm, two sub-continuum effects are expected to play a role in transistor-level thermal transport. The small region of high electric field near the drain gives rise to a small (only a few tens of nanometers across, and hence much smaller than the bulk phonon mean free path), localized hot spot. This leads to ballistic phonon transport in the vicinity of the heat source and higher temperatures than those predicted by classical diffusion theory [19][20]. In this situation, a solution to the phonon Boltzmann Transport Equation is more accurate than the classical heat diffusion equation [8].

The second sub-continuum thermal effect to be expected in ultra-scaled transistors has to do with the non-equilibrium interaction between the generated optical and acoustic phonons. Since nearly-stationary optical phonons form the majority of the vibrational modes generated via Joule heating, they tend to persist in the hot spot region until decaying into the faster acoustic modes. This non-equilibrium scenario may become particularly relevant when device switching times approach the optical-acoustic decay times, on the order of 10 picoseconds [7]. A careful transient solution of the phonon populations is necessary to properly account for the non-equilibrium distributions [22].

Both sub-continuum effects in bulk nanotransistors are expected to take place in the drain region. Hence, their effect is more likely to be pronounced on device reliability, rather than reducing the device current drive, since the latter is thought to be determined by the electron injection velocity near the source [23]. However, some indications exist that in the limit of the smallest achievable bulk silicon MOSFETs (10 nm) the optical phonons generated in the drain may reach the device source before decaying into acoustic phonons, and hence directly affect the source injection velocity [20].

THIN FILM TRANSISTORS

Thin film transistors are partially or fully depleted single-gate silicon-on-insulator (SOI) devices, planar (buried gate) dual-gate devices, or vertical FinFETs, as in Fig. 4b and Fig. 4c. They benefit from less capacitive coupling with the substrate, hence higher switching speeds, and more gate control over the channel, hence better turn-on characteristics and threshold voltage control. The sub-continuum phenomena that affect bulk nanotransistors are expected to play a much lesser role in thin film transistors. This occurs because the phonon mean free path in the thin film is strongly reduced by boundary scattering to a scale comparable to the device dimensions and the size of the drain-side phonon hot spot.

However, unlike for bulk devices, the thermal conductivity of the active device region (the thin film body) is consequently much smaller (see Fig. 5). In addition, a larger surface area to volume ratio for ultra-scaled SOI devices also implies a stronger contribution from the various materials' thermal boundary resistance. Finally, the very low thermal conductivity of the buried oxide significantly impedes heat transfer toward the substrate. Heat dissipation through the device contacts may play an important role, especially for the smallest, scaled devices. These effects are captured in the simple thermal resistance model illustrated in Fig. 6. It can be shown that device thermal properties are strongly dependent on the transistor geometry, particularly on the dimensions of the extension length L_{ex} and the raised source/drain height t_{sd} [4]. A shorter L_{ex} and taller t_{sd} are desirable from a thermal point of view, as this choice would minimize the thermal conduction path toward the device contacts. While a taller raised source/drain is also desirable from an electrical point of view (to minimize electrical series resistance), a shorter extension length can lead to significant parasitic gate-to-source capacitance, adversely affecting the switching speed of such a device. Another electrical vs. thermal trade-off exists for the thickness of the buried oxide, t_{BOX}: a thinner oxide is desirable from a thermal point of view, although electrically this would lead to higher parasitic coupling capacitance with the substrate. Similar arguments can be made about vertical FinFET devices to show that they generally have better thermal properties owing to their thicker (less thermally resistive) body, larger oxide area and overlapped gate [4]. It is clear therefore that both electrical *and* thermal considerations must be taken into account in the design of ultra-scaled future generations of thin body transistors.

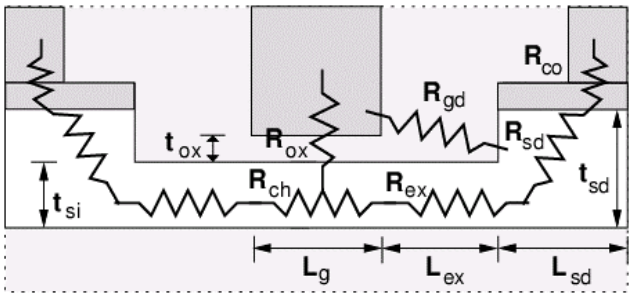

Fig. 6: Thin film transistor thermal resistance model (also see Fig. 4). The dark gray areas represent the metalized gate and contacts, the light gray is the surrounding oxide insulator [4].

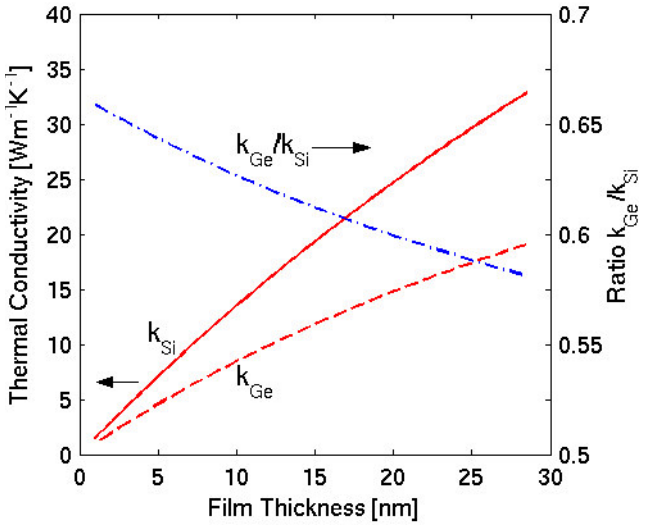

Fig. 5: Estimated silicon and germanium reduction in thin film thermal conductivity due to phonon boundary scattering alone (i.e. no confinement). Thin silicon films suffer from a stronger reduction in thermal conductivity (vs. germanium) due to the longer bulk silicon phonon mean free path [25].

GERMANIUM TRANSISTORS

Germanium field effect transistors (FETs) were largely abandoned forty years ago because germanium lacks a reliable, native insulator like SiO_2 for silicon. However, with the recent introduction of compatible high-k gate dielectrics, the existence of a viable germanium transistor has become a renewed possibility [24]. Such devices are attractive because germanium has higher low field mobility than silicon, which is thought to determine the ultimate current drive of a device [23][24]. From a thermal point of view, however, large scale integration with bulk germanium transistors is more problematic because germanium has a thermal conductivity only about 40 percent that of silicon.

On the other hand, preliminary calculations suggest that ultra-thin film germanium films take on a lesser penalty in their thermal conductivity reduction than thin silicon films, as in Fig. 5. The longer bulk phonon mean free path of silicon also implies a stronger effect of boundary scattering on the thin film thermal conductivity. As the film thickness is reduced, thin germanium films become more attractive (thermally) compared to silicon films vs. the bulk case. The thermal conductivity ratio between the two material films is also plotted in Fig. 5. The bulk thermal conductivity ratio between germanium and silicon is approximately 0.4 (Table 1), which increases to 0.65 in favor of germanium, for the thinnest films

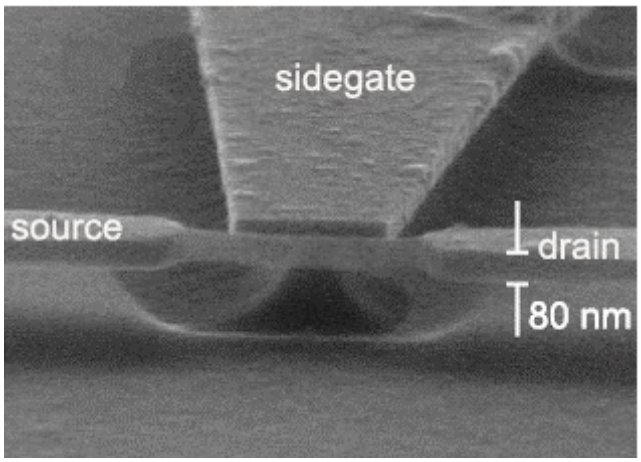

Fig. 7: Typical suspended silicon nanowire field effect device fabricated with electron beam lithography and a buffered HF underetch [28]. The cross-section of the wire is 23×80 nm. The confined dimensions significantly alter both current and heat transport through the wire.

of practical interest. Any thermal advantages thin silicon films still have over germanium could be offset by the higher mobility of the latter, possibly casting germanium-on-insulator (GOI) devices as an interesting alternative to SOI for the smallest thin film devices along the technology roadmap.

NANOWIRES

Transistors made from semiconductor nanowires have recently received a lot of attention for their current-carrying capabilities and relative ease of fabrication and integration (compared to, e.g. carbon nanotubes) with currently existing technologies [26]-[28]. Nanowires also present an ideal vehicle for studying electronic and thermal transport at nanometer length scales, as well as coupled electro-thermal transport. There are few data available on the mobility and thermal conductivity of nanowires, but it is strongly believed that confined electron *and* phonon conduction plays an important role in these devices. The theoretical understanding of such transport is still poor, and key simulation tools are not yet available.

Suspended semiconductor nanowires also represent the extreme electro-thermally confined case of a FinFET transistor or of a dual- or tri-gate device. With controlled growth on a large scale, and a solid theoretical understanding from an electro-thermal point of view, nanowires could complement (although perhaps not necessarily displace) currently existing CMOS technology.

CONCLUDING REMARKS

Traditional heat transfer research for electronic systems has focused on transport off the semiconductor chip, including air convection from the heat sink and conduction in the package. However, semiconductor roadmap (ITRS) trends and the introduction of novel device technologies may eventually cause the temperature rise on the chip, and specifically within nanoscale transistors, to approach or even eventually exceed the temperature rise between the chip and the ambient air. This situation motivates a new era of heat transfer research focused on nanoscale conduction physics, coupled electron and phonon transport modeling, and transistor design optimization. The design of any future nanotechnologies must come with a fundamental understanding of both charge and heat transport at nanometer length scales, and across various materials. The small dimensions affect both current and heat transport via quantum confinement and boundary scattering. The methods and models presented in this review are applicable beyond the silicon-based industry.

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